

Advanced Repetitive Control of Grid Converters for Power Quality Improvement Under Variable Frequency Conditions

Rabia Nazir

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ABSTRACT

Repetitive Control (RC) has proven to be an effective and efficient way of tracking/rejecting periodic signals. Periodic signals are very common in many applications like robotics, disk drive systems, power converters and many more. However, in some applications the periodic signal to be tracked/rejected has variable period, or in other words the period of the signal is uncertain. Due to the fast growing micro-processor and micro-controller technologies most of the controllers are implemented in digital domain. This thesis contributes to the topic of performance of digital repetitive control when the frequency of the reference signal is variable. A very common real life situation of continuously variable frequency signal has arisen in electrical power system due to various factors, including increasing number of distributed generators being connected to the system. The grid connected converters are influenced by this uncontrolled frequency variations. Conventional Repetitive Control (CRC) schemes always require the frequency of the reference signal to be tracked/rejected to be a constant. CRC schemes are incapable of performing well in grid connected converter systems where the grid voltage signal acts a reference signal. The contributions of this thesis can be organized as follows:

First of all, performance of the CRC scheme has been measured in terms of steady-state tracking error and Total Harmonic Distortion (THD) under time varying frequency conditions. A single-phase inverter and a three-phase rectifier has been considered to evaluate the performance of the CRC techniques. The results indicate that the CRC schemes perform well only when the frequency of the reference signal is equal to the nominal frequency and sampling frequency of the digital controller is an integer multiple of the reference frequency. This thesis is dedicated to the cases where the sampling frequency of the controller is fixed. Another approach is to vary the sampling frequency in accordance to the reference frequency variations, thus obtaining an integer ratio between the two frequencies.

An approach that overcomes the issue of CRC performance under time varying frequency conditions, when the sampling frequency of the digital controller is fixed, is by using a Fractional Order Repetitive Controller (FORC). The FORC uses a Lagrange interpolation based fractional delay filter which provides necessary non-integer delay to accomplish a sufficient condition required for tracking/rejecting a reference signal when the sampling frequency of the controller is no longer an integer multiple of the reference frequency. A design enhancement technique using optimal fractional delay filter has been proposed in order to analyze the stability and yields sufficient stability condition.

An Advanced Repetitive Controller (ARC) is used to improve the repetitive control performance under variable or uncertain frequency reference/disturbance signal conditions. It includes a Taylor series expansion based fractional delay filter to realize necessary non-integer delay. The Taylor series expansion based fractional delay filter does not need to update sub-filter coefficients even in the presence of variable frequency reference signals. Therefore, the ARC employing a Taylor series expansion based fractional delay filter is more appropriate for applications involving frequent or continuous frequency variation. It has been shown in this thesis that in case of FORC the fractional delay filter parameters vary depending upon reference signal frequency and thus may lead to system instability if the fractional delay filter used does not operate in its optimal

range. The closed-loop stability of both FORC and ARC is analyzed. Additionally, an in-depth analysis of FORC controller has been carried out to investigate the influence of every sub-system and parameters variations.

The experimental validation of FORC and ARC control schemes has been performed in two different applications: a single-phase stand-alone inverter and a three-phase grid connected PWM rectifier. The PWM rectifier is used as a grid connected converter case to analyze and show the performance of the ARC controller under frequency variations. Experimental results indicate the ARC controller is capable of achieving a near zero error steady-state tracking of a variable frequency reference signal. The performance of the ARC controller and power quality of the converter is measured and presented in terms of the THD, power factor and steady-state tracking error.

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LIST OF SYMBOLS

Repetitive Control Structure

Sampling frequency	f_s
Sampling time	T_s
Switching frequency	f_{sw}
Reference frequency	f
Reference period	T
Order of conventional repetitive controller	N_o
Low-pass filter	$Q(z)$
Compensator	$G_c(z)$
Output of repetitive controller	$u_r(z)$
Repetitive controller	$G_r(z)$
FORC repetitive controller	$G_{fr}(z)$
Phase-lead steps	m

Advanced Repetitive Controller

Integer order of the Taylor Series based repetitive controller	N_i
Sub-filters	$P_k(z)$ for $k = 0, 1, 2, \dots, M$.
Polynomial degree of each sub-filter ($P_k(z)$)	N
Taylor Series expansion based fractional delay filter	$G_t(z)$
Taylor Series based repetitive Controller	$G_{rt}(z)$
Vector containing Lagrange interpolation based sub-filters	C_t

Electrical Variables

Input Bc bus voltage	E_n
Output dc Bus voltage	U_{dc}
Three-phase ac voltages	E_a, E_b, E_c
Phase to neutral three-phase ac voltages	e_{as}, e_{bs}, e_{cs}
PWM modulated voltages	v_{ab}, v_{bc}, v_{ca}
Rectifier load resistance	R_r
Rectifier load capacitance	C_r
Rectifier load inductance	L_r
Nominal filter inductance	L_n
Nominal filter capacitance	C_n
Back <i>emf</i> of load	E_l
Ac-side line currents	i_a, i_b, i_c
Capacitor current	i_c
Peak value of input ac-side current	I
Peak value of input ac-side voltage	E
Output load voltage of the single-phase inverter	v_c
Output load current of the single-phase inverter	i_o
Output current of single-phase inverter	i_l

FD Filter Variables

Order of FD filter	n
Fractional delay	F
Lagrange interpolation based FD filter co-efficients	$A_k, k = 0, 1, 2 \dots$
Fractional delay filter	$G_f(z)$

General Symbols

Conventional controller	$G_x(z)$
Plant	$G_p(z)$
Error	$e(z)$
Integral gain	k_i
Proportional gain	k_p
Change in reference frequency	Δf
Nyquist frequency	f_N, ω_N
IGBT switching signals	S_1, S_2, \dots, S_6
Switching function of three legs of converter	S_j where $j = a, b, c, S_j = \pm 1$
Non-linear rectifier load diodes	D_1, D_2, \dots, D_4
Modulation index	D_i
On time of a pulse in k^{th} sampling interval	$t_{j+}(k)$
Parameters of low-pass filter $Q(z)$	α_0 and α_1
Converter parameters variations	$\Delta L, \Delta C, \Delta R$

Abbreviations

Advanced Repetitive Control/Controller	ARC
Alternating Current	ac
Auto Regressive Moving Average	ARMA
Band Width	BW
Conventional Repetitive Control/Controller	CRC
Conventional Repetitive Controller Using Nominal Integer Order	CRC _N
Conventional Repetitive Controller Using Truncated Integer Order	CRC _T
Digital Signal Processor	DSP
Direct Current	dc
Discrete Fourier Transform based RC	DFT-RC
Distributed Generator	DG
Feedback Controller	FC
Finite Impulse Response	FIR
First Input First Output	FIFO
Fractional Delay	FD
Fractional Order Repetitive Control/Controller	FORC
Fractional Order Repetitive Controller using Optimal FD	FORC _O
Frequency Adaptive Hybrid Selective Harmonic Control	FA-SHC
Gate Turn Off Thyristor	GTO
Graphical User Interface	GUI
Infinite Impulse Response	IIR
Internal Model Principle	IMP
Internal Model Principle based Selective Harmonic Control	IMP-SHC
Insulated Gate Bipolar Transistor	IGBT
Iterative Learning Control	ILC
Metal Oxide Semi-conductors Field Effect Transistor	MOSFET
Multiple Resonant Controllers	MRSC
One Sampling Ahead Preview	OSAP
Proportional Integral	PI
Pulse Width Modulation	PWM
Repetitive Control	RC
Resonant Control/Controller	RSC
Selective Harmonic Control/Controller	SHC
Total Harmonic Distortion	THD

Chapter 1

INTRODUCTION

The electrical energy crisis and environmental problems caused by the use of fossil fuels (oil, coal and gas), have led the power industry to look at renewable energy resources as a supplement to meet energy demand. To secure a clean, sustainable and economical power supply, electricity networks are undergoing a significant evolution from centralized, long transmission lines and traditional systems to ‘Smart Grids’ with a high penetration of renewable Distributed Generators (DGs) within distribution systems [1–6]. Since DGs are near the utilization point, distributed generation can reduce transmission line losses. More and more large-scale renewable generators (solar, wind and others) acting as power plants are also connected directly to the transmission networks [4, 7, 8]. As the grid penetration and power level of these plants increase steadily, it starts to have significant impacts on the power system. Therefore, more advanced generators, power electronic systems, and control solutions need to be introduced to make these plants more suitable to be integrated into the power grid [9].

Power electronics is the key enabling technology for renewable energy source control and its integration with load [10, 11]. High-efficiency smart power electronic systems can precisely convert, control and condition electricity [12]. Power electronic interfaces (*i.e.* grid converters) enable high penetration of DGs into the electricity grids [13–17]. Grid converters offer quite flexible power conditioning functionalities. With an increased level of grid converter interfaced DGs, power distribution networks can be transformed into flexible, interactive, bidirectional smart grids that distribute electricity more efficiently. Figure 1.1 shows how the grid converters provide an efficient interface between the DGs and power system. In grid connected mode, grid converters feed active/reactive power from DG to the grid while voltage and frequency is imposed by the grid. Grid converter based integration of DGs significantly affects the overall performance and stability of the grid. Therefore, there is a need to develop grid converters with well designed functionality.

Control technology underpins the power conditioning functionalities of grid converters, and consequently influences and even determines the stable, secure and reliable operation of the grid [10, 18–20]. Power conditioning contains harmonic filtering, harmonic damping, harmonic isolation, harmonic termination, reactive power control for power factor correction, power flow control, voltage regulation, load balancing, voltage-flicker reduction and/or their combinations. Instantaneous active and reactive power theory, also known as ‘p-q theory’, is based on the set of instantaneous powers defined in the time domain, and is applied in designing power conditioning circuits.

To suit power system specifications, high performance control strategies are required for the grid converters to regulate voltages, currents and/or frequencies with minimum steady-state error, while maintaining fast transient response, guaranteeing robustness and being feasible in practice. In other words, high performance control strategies need to be accurate, fast, robust and implementable. Since the fundamental electrical signals (voltage and current) of the power system are periodic ac signals, an associated control issue is how to exactly track periodic

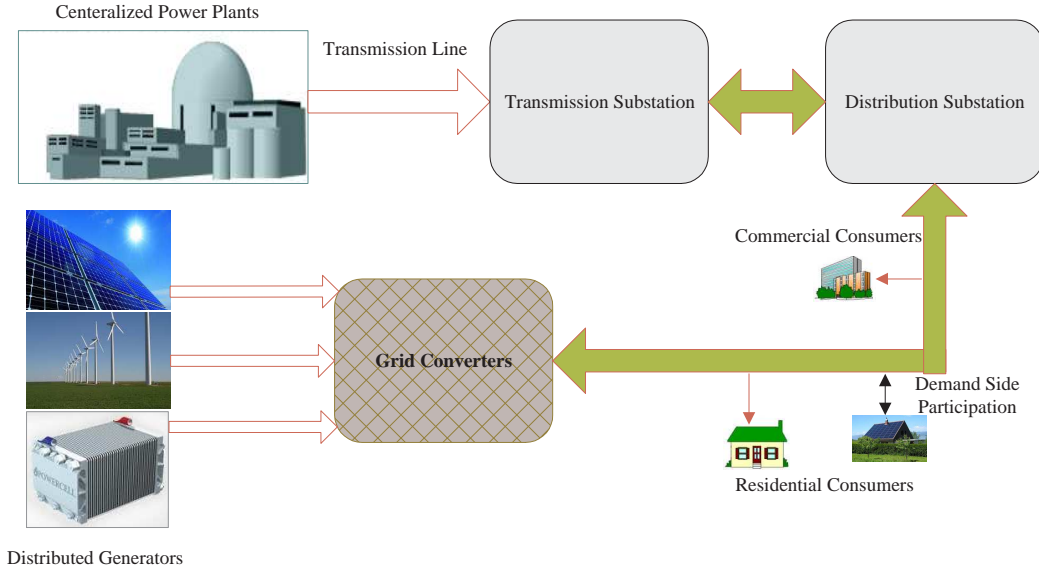


Figure 1.1: A simple grid connected distributed power generation system.

signals. This research develops an Advanced Repetitive Controller (ARC) for the grid connected converters in a continuously time varying frequency environment.

1.1 BACKGROUND

With the development of fast-switching power devices, Digital Signal Processors (DSPs), micro-controllers and control technologies, many attempts have been made to develop advanced control strategies for power converters, such as synchronous-frame Proportional Integral (PI) control [21–25], predictive control [26–29], sliding mode control [30–35] and hysteresis control [36–38] *etc.* However, a synchronous-frame PI controller can only regulate sinusoidal fundamental frequency signals and it best suits three-phase converters, since the implementation of synchronous reference frame regulators requires a minimum of two independent phases in the system. In some cases a second phase for implementation is constructed by applying a 90° phase shift with respect to the fundamental frequency of single-phase signal [25]. Predictive controllers have a straightforward design procedure for both linear and non-linear models but their performance is dependent on an accurate model and is very sensitive to uncertainties and disturbances [27]. The random switching patterns of sliding mode and hysteresis control may lead to difficulty in low-pass filtering and over-stress on switching devices and microprocessors. Thus, these control schemes fail to provide a satisfactory control solution to power converters.

In the 1970s, Francis and Wonham summarized the Internal Model Principle (IMP): it states that perfect asymptotic rejection/tracking of a persistent input can only be attained by replicating its signal generator (internal model) in a stable feedback loop [39–46]. The internal model simulates the response of the system (plant) in order to estimate the outcome of a system command. Both the Repetitive Controller (RC) and Resonant Controller (RSC) are based on the IMP. IMP based controllers handle three types of situation and modify the feedback control system with the aim to achieve zero steady-state tracking error of the reference signal. These are:

- When the aim is to track a reference or command signal which is periodic.
- When the desired output signal is a constant dc but there is a periodic disturbance, and the aim is to cancel/reject the periodic disturbance and achieve a constant dc output.

- When both the desired output and the disturbance signal are periodic and possess the same frequency, and the aim is to achieve a zero steady-state tracking error of a periodic reference in the presence of periodic disturbance.

Any periodic signal can be decomposed into its fundamental frequency component and an infinite number of harmonic components. Classical control techniques enable us to compute the steady-state frequency response to each of these frequencies. However, practically it is not possible to accommodate infinite harmonic frequencies so a compromise is made and zero steady-state error is achieved up to some chosen cutoff frequency only, usually the Nyquist frequency. RC and RSC can precisely track/reject periodic reference/disturbance waveforms with zero steady-state error. Since the grid electrical variables (voltage and current) are periodic, the internal model principle based periodic control techniques (RC & RSC) provide promising high performance control methods for grid converters. Periodic control schemes (RC & RSC) are widely employed to control grid converters.

Based on the IMP, a resonant controller can achieve exact tracking of a sinusoidal signal by including its generator in a closed-loop system [46]. To reduce Total Harmonic Distortion (THD), a parallel combination of Multiple Resonant Controllers (MRSC) can be used to eliminate corresponding harmonics [47, 48]. The parallel structure enables MRSC to have independent gain for each resonant control component to achieve quite fast transient response. However, if the number of resonant control components is large, MRSC may cause a heavy computation burden and parameter tuning difficulty [47]. Due to its simplicity and effectiveness, RSC has become a popular current regulator for grid converters [43, 46–50].

Also based on the IMP, RC can achieve zero steady-state error for the control of arbitrary waveform periodic signals but with slow dynamic response, whereas RSC is faster but rejects only single-frequency components [47, 48]. RC is equivalent to a parallel combination of a PI controller and RSC components at all harmonic frequencies [43, 47, 49]. These RSC components enable RC to reject all harmonics, by providing exactly same but very high gains at all harmonic frequencies (also called resonant frequencies). Its recursive form enables RC to consume much less computation than MRSC does. However, since the gains for all RSC components of RC are equal, it is impossible for RC systems to have an optimized transient response. RC usually yields much slower transient response than MRSC does, since the control gain at all harmonic frequencies are same.

To make a good trade-off between accurate but slow RC and high computational burden but fast RSC, Selective Harmonic Control (SHC) has been invented to regulate the featured $nm \pm k$ order harmonics of grid converters [51]. SHC is also called selective harmonic RC, which is compatible with RC. RC, RSC and SHC are periodic control strategies that offer a high performance control solutions for grid converters [47].

1.2 MOTIVATION AND PROBLEM STATEMENT

In most applications, repetitive control is implemented in the discrete domain. That is, the computations are performed at certain instants of time only (*e.g* at $T_s, 2T_s, 3T_s, \dots$) and the signal generated by the repetitive controller is a discrete time periodic signal. It requires that the ratio of the sampling frequency ($f_s = 1/T_s$) to the reference signal frequency (f) should be integer so that the number of samples per reference signal period is an integer. The frequency of the electrical power system is becoming more and more fluctuating because of the intermittent DG systems. Therefore, in the case of grid connected converters, the ratio of the sampling frequency to the grid frequency cannot always maintain an integer value, as the grid frequency is varying due to temporary imbalance between the load and generated power and many other factors. According to the grid code for DGs in New Zealand, a frequency band between 49.8 Hz and 50.2

Hz (both inclusive) is known as normal frequency band and the extreme grid frequency variation range is up to (± 5 Hz) except for momentary events [52]. During momentary fluctuations frequency stays between 47 Hertz and 52 Hertz (both inclusive) and system operators restore the frequency to the normal band as soon as reasonably practicable having regard to all the circumstances surrounding the fluctuation [52]. The normal frequency band and momentary fluctuations can cause the ratio of sampling to reference frequency become non-integer. The non-integer samples would cause the resonant frequencies of a repetitive controller to deviate from the grid frequencies (fundamental and harmonics). That is to say, RC cannot exactly track or reject periodic signals of grid frequencies. As a result the grid converters inject inter-harmonic currents into the grid, and cause power-flow oscillations. Non-integer number of samples per period degrades the power quality, and even may affect the normal operation of the grid.

To avoid the issue created by varying grid frequency, variable sampling rate RC or RSC can be used. However, variable sampling rate method is seldom used due to its complexity, among other reasons. Preliminary research results show that fractional-period repetitive control technology could effectively deal with fractional period or variable frequency periodic signals. In [53], an adaptive repetitive control has been developed to track a variable period signal with fixed sampling time. Rashed *et al.* [49] proposed a similar method for three-phase grid inverters, which used estimated grid frequency to adaptively update RC period and RSC resonant frequency while interpolation is used to preserve the RC rejection capability under non-integer samples per period. On the other hand, fractional delay based repetitive control schemes can be used, where a fractional delay low pass filter is introduced to approximate the internal model (signal generator) of fractional-period signals [54, 55]. Two different methods have been used to design fractional delay low-pass filters: Lagrange interpolation method and least square method. However, the current Fractional Delay (FD) filter based control methods redesign the low-pass fractional delay filter every time the frequency of the reference signal varies. Continuously redesigning a filter in a control system may lead to destabilization of the system.

To always ensure high performance repetitive control of grid connected converters, an advanced unified fractional-period repetitive control technology is needed.

1.3 AIMS AND OBJECTIVES

This thesis contributes to the topic of “performance of repetitive control working under variable frequency reference signals”. In preliminary research work, a single-phase inverter and a three-phase PWM rectifier have been simulated using conventional repetitive control schemes when the frequency of the reference signal is varying (Chapter 2). The simulation results indicate that the conventional RC schemes are unable to track a reference signal of variable frequency as the steady-state tracking error is significantly high. Therefore, the aim of this research is to develop an advanced periodic control technology to deal with periodic signals of time-varying frequencies, and consequently enable grid converters to exactly track periodic voltages or currents for better power quality and power conditioning. The objectives of this research work are:

- Modeling of grid converter based systems, such as single-phase and three-phase inverters for DGs (PV, wind turbine and fuel cell etc) and power rectifiers for loads.
- Implement and test repetitive control strategies and their implementation under variable system frequencies.
- Propose and develop new control strategies to allow high performance and computationally efficient converter control (RC and/or RSC) under non-nominal system frequencies.
- Assess performance of new control strategies by simulation and experiments.

1.4 CONTRIBUTION

The contribution of the thesis can be organized as follow:

- **Analysis of recently developed repetitive control methods working under variable frequency reference signal conditions.** The performance of conventional digital repetitive controllers is investigated under variable frequency conditions. It is shown in this thesis that the performance of the digital repetitive controllers strongly depends upon the ratio of sampling frequency to the reference signal frequency and performance degrades drastically when the reference signal frequency varies from its nominal value. The fractional delay based repetitive controller structure and its performance are also analyzed.
- **Design methods for advanced repetitive controllers dealing with variable frequency conditions.** A Taylor series expansion based digital repetitive controller design is presented in the thesis. This controller is able to perform well under variable frequency conditions and does not require any changes or updates in the filter structure. A detailed design and analysis of a Taylor series expansion based digital repetitive controller is systematically presented.
- **Stability and robust performance analysis of the advanced repetitive controller.** Stability and robustness analysis of the advanced repetitive control are carried out to prove the effectiveness of the controller. Transient response, steady-state error, harmonic rejection capability and frequency adaptive capability are also analyzed.

1.5 OUTLINE

Chapter 1 presents basic introduction, motivation, problem statement and contribution of this research work. Chapter 2 describes most commonly used grid converter control techniques, basics of repetitive control and detailed analysis of the performance of conventional repetitive control scheme when the frequency of the reference signal is variable. Chapter 3 describes the design and development of a test rig used to carry out all the experimental investigations throughout this research work. This Chapter also provides the details of the equipment used. The state-of-the-art research in the field of RC is presented in Chapter 4. It also presents contribution to the design of Fractional Order Repetitive Controller (FORC) and stability analysis of FORC controlled systems. A novel control scheme named Advanced Repetitive Control (ARC) has been proposed in Chapter 5. A systematic design methodology and stability conditions have been presented in this chapter. The ARC performance has also been verified and compared to FORC performance in this Chapter. Chapter 6 presents the experimental verification of ARC controller for grid connected converters. A three-phase PWM grid connected rectifier is used as a plant in this chapter. Finally, conclusion and suggested future work are presented in Chapter 7.

Chapter 2

GRID CONVERTER CONTROL TECHNIQUES AND REPETITIVE CONTROL

2.1 INTRODUCTION

This Chapter describes the most commonly used control techniques for grid connected converters. Since the reference signal to be tracked in case of grid connected converter is periodic, special attention has been paid to control approaches that are primarily used for periodic processes. The control methods, which play an important role in controlling repetitive or periodic processes, are known as learning controllers. Repetitive Control (RC) scheme is a branch of learning control. Basic concepts of RC are described in this Chapter. The performance of RC control under time varying frequency conditions is also presented and analyzed here. Two different systems, a single-phase Pulse Width Modulation (PWM) inverter and a three-phase PWM rectifier, demonstrate how the performance of an RC controller degrades under variable frequency conditions. Thus a need for an Advanced Repetitive Controller (ARC) which is capable of performing equally well in variable and fixed frequency conditions is shown.

This Chapter is organized as follows: Section 2.2 briefly describes some of the most commonly used control techniques, including RC, for control of power converters. Section 2.3 gives basic information and insight into the repetitive control concepts. Section 2.4 analyses the performance of Conventional Repetitive Control (CRC) schemes under varying frequency conditions and finally Conclusion are presented in Section 2.5

2.2 CONTROL TECHNIQUES FOR GRID CONNECTED CONVERTERS

The main functionality of grid connected voltage source converters is to synchronize and transfer the variable generated power to the grid. A linear or non-linear control algorithm can be selected for the operation of the grid connected converters. Figure 2.1 shows a very basic block diagram of a grid connected converter system. The controller block is responsible for taking in the actual and reference signals and producing the correct PWM signal which can reduce the tracking error in upcoming periods. The criterion for the selection of the appropriate control scheme usually involves a trade-off between cost, complexity, and quality. This Section summarizes some of the previously reported control approaches for grid connected converters and their impact.

2.2.1 Proportional Integral Control

The Proportional Integral (PI) controller provides an infinite gain for the dc component, thus guaranteeing the system to track a dc reference without any steady-state error. Unfortunately, for ac signals a simple PI controller provides steady-state error due to the finite gain at the frequency of interest [56, 57]. However, synchronous reference frame PI controllers can track

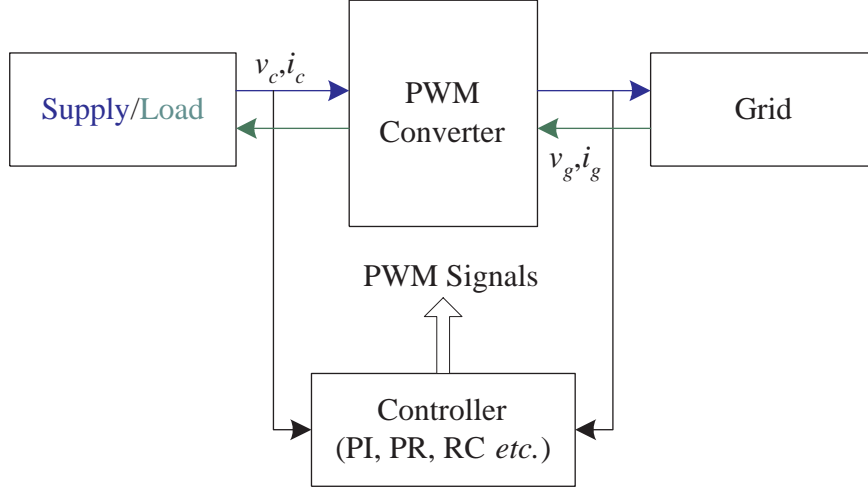


Figure 2.1: Block diagram of a grid connected converter system.

ac signals and have been successfully used in grid connected converters [3, 21, 48, 58, 59]. In synchronous reference frame the ac signals at fundamental frequency are transformed to the Synchronous Reference Frame (SRF) ($abc \rightarrow dq$). This transformation results in two stationary signals as the synchronous reference frame synchronously rotates with the reference signal. Thus the control variables become stationary values which can be easily controlled using PI controller with zero steady-state error. For single-phase grid connected converters employing a synchronous reference frame PI controller a fictitious second phase is generated to allow emulation of a two-phase system for transformation to dq axis.

The major concerns with the synchronous reference frame PI controller are its high complexity and computational burden because of the ($abc \rightarrow dq$) transformation, very high sensitivity to noise, error in synchronization, and indirect and computationally more complex application to single-phase systems [60, 61]. Proportional Resonant (PR) controllers are considered to be equivalent to conventional PI controllers implemented in two synchronous reference frames at the same time: one positive-sequence SRF and one negative-sequence SRF [24, 61]. PI control works with system variables referred to a stationary frame whereas with PR controllers, the PI control characteristics are transformed to the system frequency.

2.2.2 Proportional Resonant Control

Proportional Resonant (PR) controllers have been widely used to provide precise tracking of periodic and highly complex reference waveforms in many applications [18, 22, 40, 46, 48, 49, 62]. The idea of PR controllers is based on the Internal Model Principle (IMP) where zero steady-state tracking error is achievable if the model of the periodic reference signal is part of a stable closed-loop system. The IMP is explained in detail in Section 2.3. The transfer function of an ideal PR controller ($G_{PR}(s)$) is given as [46]:

$$G_{PR}(s) = k_p + \frac{k_r s}{s^2 + w_o^2} \quad (2.1)$$

where k_p and k_r are proportional and resonant control gain, and w_o is the nominal fundamental frequency of the reference signal. Eq. (2.1) gives infinite gain at the ac frequency of w_o , and insignificant phase shift and gain at other harmonic frequencies. The proportional gain k_p is tuned in the same way as for a PI controller, and it basically determines the dynamics of the system in terms of bandwidth, phase and gain margin. Thus PR control is known to reject a

single-frequency component with fast dynamic response. However, multiple parallel structure PR controllers have also been used to reject multiple harmonics of the reference signal [40, 48] but the computational complexity of multiple parallel structure PR controller is very high. Although PR control alleviates some of the shortcomings associated with PI control, but it is still only feasible for selective harmonic compensation.

2.2.3 Sliding-Mode Control

The sliding-mode control structure was first proposed in the 1950s. Essentially, a sliding-mode control system utilizes a switching control law to drive the state of the concerned non-linear plant/system to a pre-designed curve (also called the sliding curve) in the state-space, and then keep the plant's state trajectory sliding over that curve in the subsequent time [34, 35]. The sliding-mode strategy provides a systematic approach to the problem of maintaining stability and performance in the presence of modelling uncertainty [33]. The most distinguished feature of a sliding-mode control system is its insensitivity to parametric uncertainty and external disturbances. Therefore, the sliding-mode control scheme has been used for the closed-loop control of power converters under huge load variation. The sliding-mode control structure can be implemented in both analogue and discrete domains. Analogue realization results in higher stress of the switching devices and more complicated hardware. Microprocessor based realization can reduce the hardware complexity of the sliding-mode controller [33]. However, since the design methodology of analogue sliding-mode control structure cannot be directly extended to discrete-time implementation, the sampling action of the microprocessor may bring chattering or instability to the system. The digital sliding-mode control structure has shown good transient characteristics as load varies, but the steady-state response is poor [32, 33]. A pure sliding-mode controller has following disadvantages; chattering (oscillations in the system switchings above and below the required switching trajectory), sensitivity, and difficulty of equivalent dynamic formulation.

Sliding-mode control needs the optimum sliding curve selection for a given cost function and the design of a switching control that will drive the plant state to the switching surface and maintain it on the surface upon interception. A Lyapunov approach is used to characterize this task.

2.2.4 Periodic Control Techniques

Periodic processes perform the same task over and over again. Examples of the periodic systems may include robot arm manipulators, chemical batch processes and reliability testing rigs [45, 63]. All of these systems are required to perform the same action over and over again with very high precision. Thus, the required action is actually accurate tracking of a periodic reference signal $y_{ref}(t)$.

Periodic control techniques, also known as learning control techniques, work repeatedly and repetition enables the system to improve tracking accuracy from one repetition to another. These techniques learn the behavior of the system in one repetition or trial and use that information to reduce tracking error or enhance tracking performance in next repetition [45, 63–67]. Commonly used periodic control schemes in the literature are discussed below.

Iterative learning control

Iterative Learning Control (ILC) is primarily focused on processes that are executed repetitively. The ILC approach resets the system to the same initial condition before each run. The ILC approach observes the input and error generated in the current repetition and then uses this information to make adjustments to the input for the next repetition to reduce the error. This is

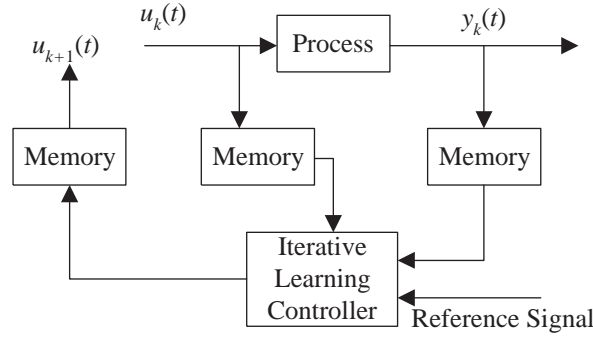


Figure 2.2: Block diagram of an iterative learning controller.

shown in Figure 2.2, where $u_k(t)$, $u_{k+1}(t)$ and $y_k(t)$ are input to the process in current and next sampling period and output of the process in current sampling period respectively [41, 63–65]. This feature differentiates ILC from conventional control approaches where error information is not fed back from one repetition to the next. The ILC control technique is considered to be a sister approach to RC. There are many similarities but certain differences between these two. One major difference is that ILC assumes a fixed initial condition for the system at the start of each iteration whereas RC updates the initial condition as a result of input action in the previous cycle. This makes the stability condition for the two controllers significantly different. Recently, the ILC approach has been successfully used in the control of grid connected converters [68, 69].

Repetitive control

Repetitive control is another widely used technique for the control of periodic processes. Just like ILC, RC control technique also updates the control signal for the next iteration by observing the error in current iteration. However the initial condition is updated after every iteration. RC control is explained in detail in Section 2.3.

2.3 FUNDAMENTALS OF REPETITIVE CONTROL

2.3.1 The Internal Model Principle

The internal model principle states that the output of a closed-loop system can track/reject the reference/disturbance signal with zero steady-state error if an accurate realization (model) of the reference/disturbance generator is included in that stable closed-loop system [43, 47, 53, 64, 67, 68]. The realization or model of the reference/disturbance signal is commonly known as “internal model” in control theory.

Signals with a dc content can be modelled by using an integrator. An integral action in the feedback loop reduces the steady-state error for constant reference and/or disturbances to nearly zero. A discrete-time integrator can be modelled as a unit delay with a positive feedback as shown in Figure 2.3 [42, 66]. In other words only one memory location is needed to store the integral value.

Similarly, periodic signals can be modelled by a memory loop which generates an output at frequencies $k\omega$, with $k = 0, 1, 2, 3 \dots$ and ω being the angular frequency of the periodic signal [42, 66]. In a memory loop, a signal with period $T = 2\pi/\omega$ is stored in a First In First Out (FIFO) buffer. The ratio of the signal period T and sample period T_s defines the number of memory

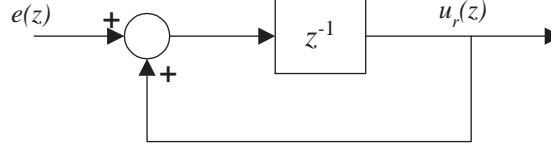


Figure 2.3: Block diagram of a discrete integrator.

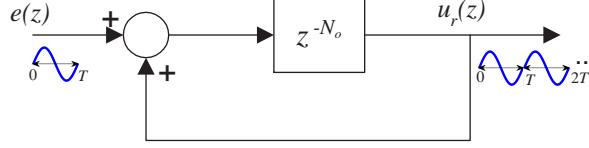


Figure 2.4: Block diagram of a standard memory loop in discrete domain.

locations needed. For example, if the period of the reference signal is 0.02 s (*i.e.* $T = 0.02$ s, $f = 50$ Hz) and sample period $T_s = 0.2$ ms ($f_s = 5$ kHz) then $T/T_s = 100$ memory locations would be needed to store the reference signal. If a positive feedback is established from output of FIFO buffer to its input, in the steady-state no input is needed to generate an output with time period T . The periodic signal at the output of FIFO buffer has a discrete frequency spectrum with peaks at $k\omega$. A block diagram of a standard memory-loop in discrete domain with time period T is shown in Figure 2.4 [42, 66]. The transfer function of a standard memory loop shown in Figure 2.4 is given as:

$$\frac{u_r(z)}{e(z)} = \frac{z^{-N_o}}{1 - z^{-N_o}} \quad (2.2)$$

where $N_o = T/T_s \in \mathbb{N}$.

Notice that (2.2) has poles around $k2\pi f$ where $k \in \mathbb{N}$. Thus zero tracking error in closed-loop is ensured if the close-loop system is stable. Figure 2.5 shows a magnitude response of the internal model given by (2.2) when $f = 50$ Hz and $f_s = 5$ kHz *i.e.* $N_o = 100$. It can be noticed that the response presents very high gain at fundamental and harmonic frequencies below the Nyquist frequency (*i.e.* $5000\pi = 15708$ rad/s in this case). The highest peak towards the end marks the Nyquist frequency. In this case, fifty harmonic frequencies exist below the Nyquist frequency and high gain is obtained at all these harmonic frequencies.

2.3.2 The Repetitive Controller

Repetitive controllers can be decomposed into three main parts; the internal model ($z^{-N_o}/(1 - z^{-N_o})$), low-pass filter ($Q(z)$) and the compensator ($G_c(z)$). The internal model is primarily in charge of ensuring zero steady-state error, the low-pass filter enhances the system robustness while the compensator guarantees the stability of the closed-loop system [70]. Three different structures (ordinary RC structure, feed-forward RC structure, plug-in RC structure) have been used in the literature to implement RC [66]. However, the plug-in repetitive control structure (Figure 2.6) has been used throughout this research work. The repetitive controller is used to augment an existing conventional feedback controller ($G_x(z)$). The feedback controller is designed to stabilize the plant ($G_p(z)$) and provides disturbance attenuation across a broad frequency spectrum.

Now the purposes served by the main parts of the RC controller are discussed in detail and then the structures used to implement RC are explained.

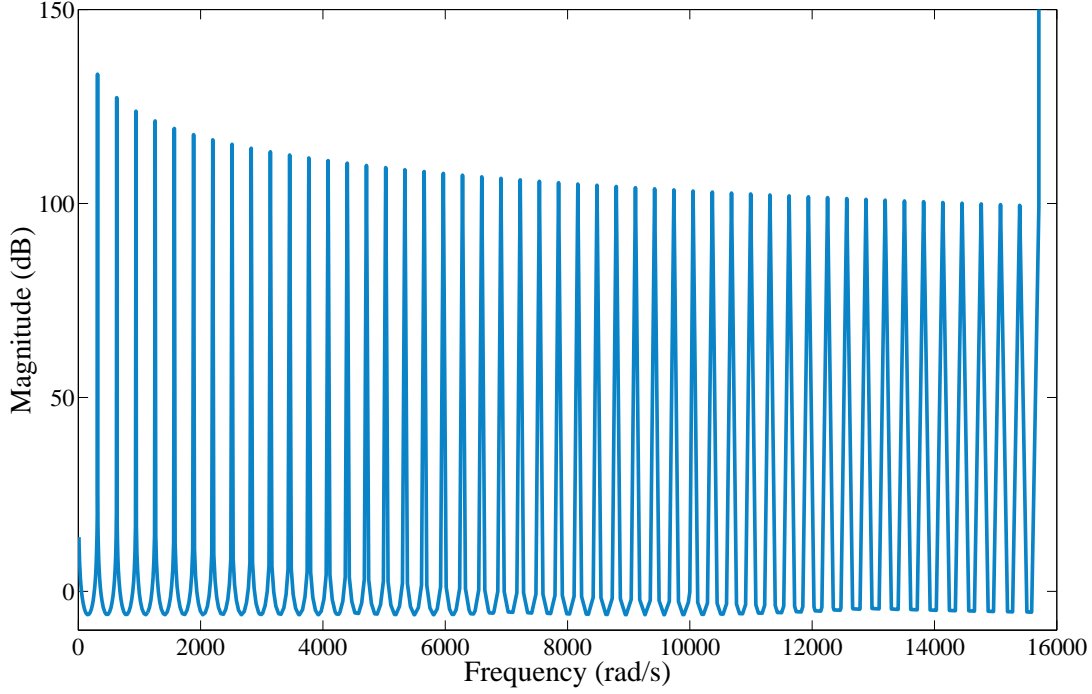


Figure 2.5: Frequency response of a standard memory loop or periodic signal generator when $f = 50$ Hz and $f_s = 5$ kHz.

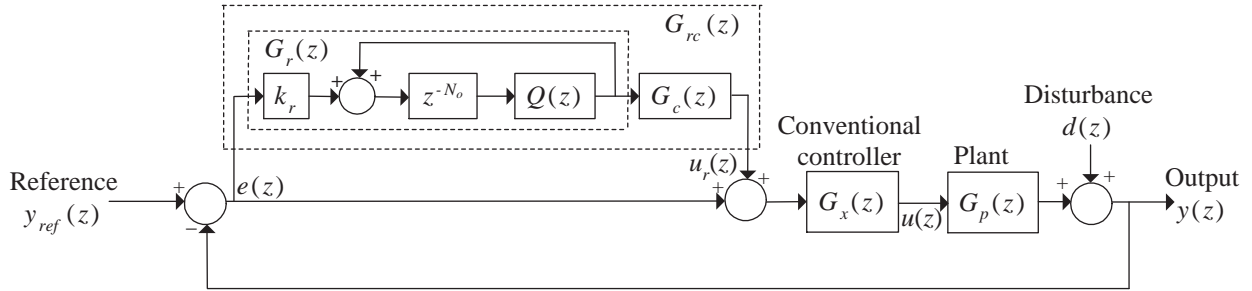


Figure 2.6: Block diagram of discrete time RC control system.

Internal model

The direct implementation of the internal model $(z^{-N_o}/(1 - z^{-N_o}))$ is often unstable. Therefore there is a need to stabilize the internal model first. Figure 2.7 shows a pole-zero plot of an internal model for $N_o = 50$. It can be seen that location of all these 50 poles is on the unity circle. Therefore, the internal model by itself is very critically stable and slight variation in parameters lead to unstable operation. In practical implementations it is often unstable.

To stabilize the internal model various modifications in the internal model have been suggested in the literature. One way to achieve this is by using a low-pass filter in series with the delay line z^{-N_o} which unfortunately compromises the rejection of higher order harmonics. However it is impossible to stabilize the whole system (plant and controller) using an internal model. Therefore, a conventional feedback controller, represented by $G_x(z)$, is used to stabilize the plant over a wide frequency range.

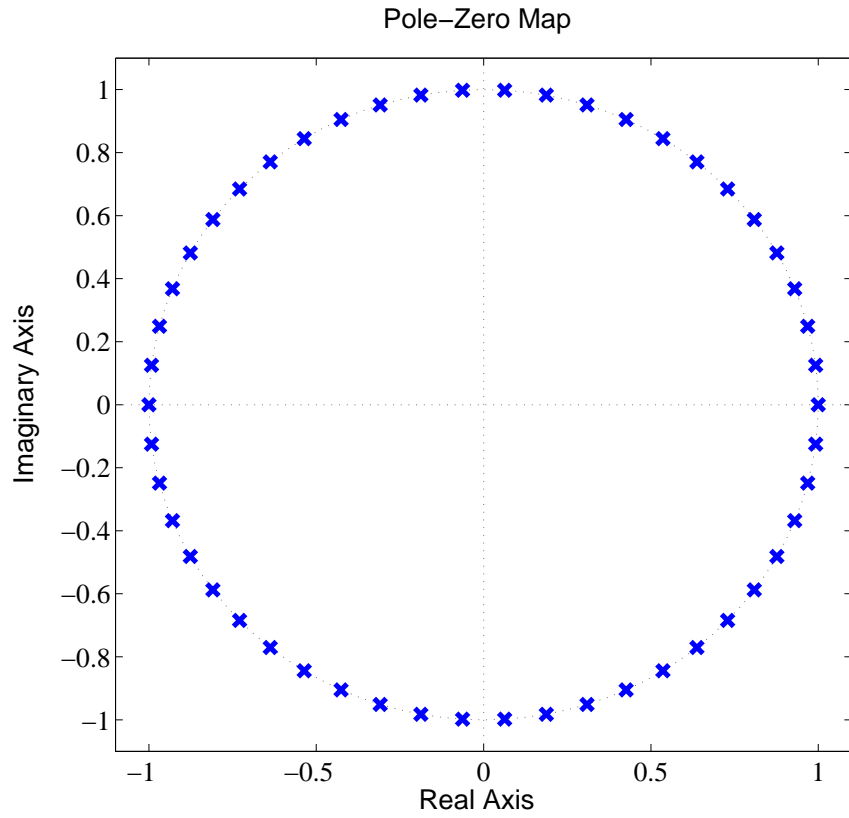


Figure 2.7: Pole-zero plot of an internal model ($z^{-50}/(1 - z^{-50})$) showing all the poles on the boundary of the unity circle.

Low-pass filter

A linear phase first order low-pass filter ($Q(z)$) of the form $\alpha_1 z^{-1} + \alpha_0 + \alpha_1 z^1$ where $2\alpha_1 + \alpha_0 = 1$ is commonly used to suppress higher order harmonics rejection capability and thus achieving stability of the internal model. The frequency response of the low-pass filter needs to be unity in the low frequency range where the tracking of the signal is very important and nearly zero outside the bandwidth of the filter so as to improve the stability of the system (internal model and low-pass filter). Figure 2.8 shows the frequency response of various $Q(z)$ filters. It is clear that the bandwidth of the filter is directly proportional to α_0 .

Figure 2.9 indicates the pole-zero plot of the internal model with various low-pass filters, whose frequency response has been shown in Figure 2.8. The system for Figure 2.9 is $\frac{z^{-50}Q(z)}{1 - z^{-50}Q(z)}$. It is difficult to see the exact pole location from these pole-zero plots due to their small scale. However the exact pole location has been checked using long format in MATLAB and it showed that all poles now lie inside the unity circle except the one at $z = 1 + j0$. It can also be concluded from Figures 2.8 and 2.9 that a low-pass filter brings a trade-off between the stability and higher order harmonic rejection. The $Q(z) = 0.05z^{-1} + 0.9 + 0.05z^1$ has the highest bandwidth among the three low-pass filters under consideration and this brings the least stability to the overall system as the poles of the system lie close to the boundary of the unit circle.

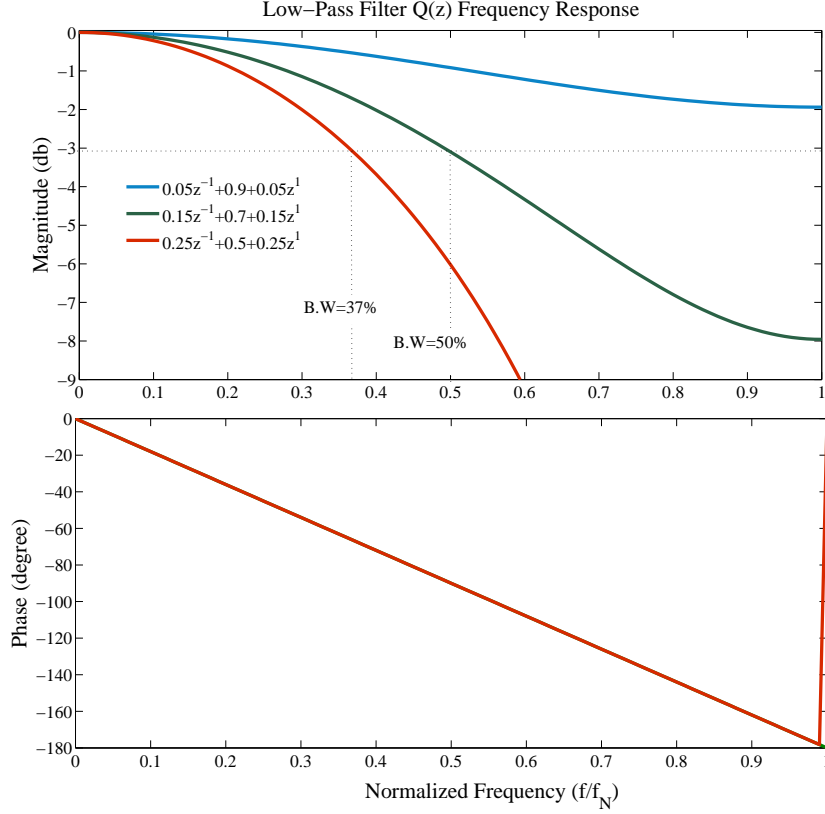


Figure 2.8: Frequency response of various low-pass filters $Q(z)$.

Compensator

The compensator $G_c(z)$ is an implementation of the zero phase error tracking controller. For the design of RC system $G_c(z)$ is best chosen as the inverse of the system model to achieve zero phase error tracking. However, practically the plant model $G_p(z)$ contains unmodelled dynamics and parameter uncertainties, thus it is impossible to implement the inverse model of the converter system. Consequently it is hard to achieve zero phase error tracking control.

In [45, 71] a simple phase-lead concept has been introduced by employing a lead step m as a compensator in the repetitive control law. Appropriate value of lead step m is usually found by experiment. Therefore $G_c(z)$ is designed as:

$$G_c(z) = z^m \quad (2.3)$$

In the frequency domain, a lead step m introduces a phase lead to compensate for phase lag, especially at high frequencies. In addition, it can also compensate for unknown time delays, which are not modeled. Such a lead step m will produce a linear phase lead

$$\theta = m \frac{\omega}{\omega_N} 180^\circ \quad (2.4)$$

at a frequency ω , which reaches $m \times 180^\circ$ at the Nyquist frequency ω_N .

Ordinary RC structure

The main parts of the RC controller can be same for all three structures but there are some differences in implementation and performance (*e.g.* RC gain, parameter values and stability

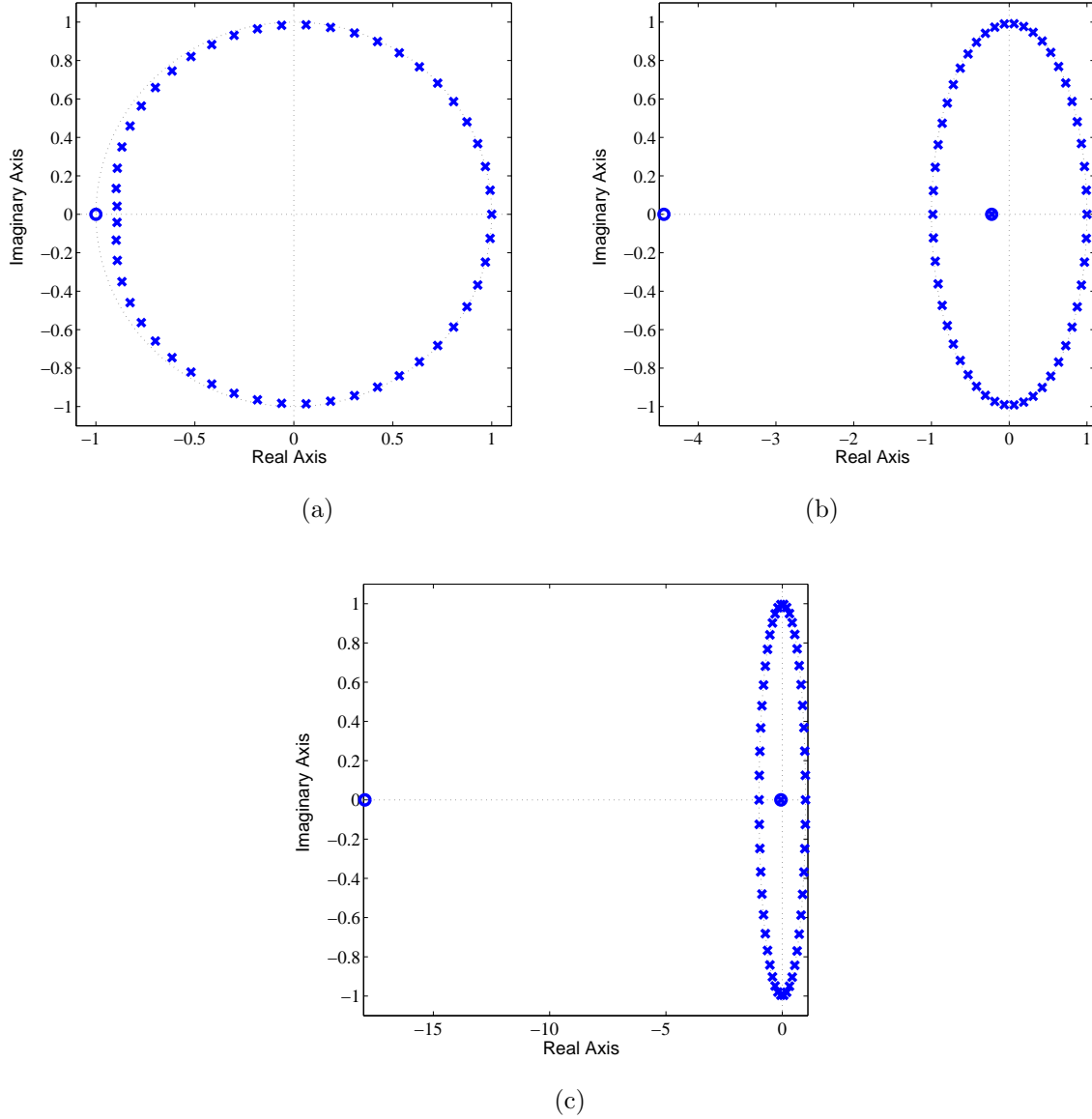


Figure 2.9: Pole-zero plot of an internal model $(z^{-50}/(1 - z^{-50}))$ along with various $Q(z)$ filters: (a) $Q(z) = 0.25z^{-1} + 0.5 + 0.25z^1$ (b) $Q(z) = 0.15z^{-1} + 0.7 + 0.15z^1$ (c) $Q(z) = 0.05z^{-1} + 0.9 + 0.05z^1$.

range). In the case of the ordinary RC structure, the whole control system is modified to include RC ($G_{rc1}(z)$) and RC controller adjusts the command to a feedback control system as shown in Figure 2.10 [66].

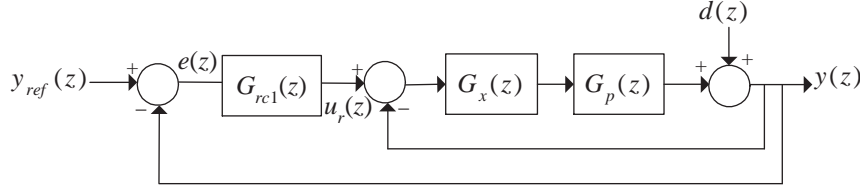


Figure 2.10: Ordinary RC structure adjusting the command to a feedback control system.

Feed-forward RC structure

In the case of feed-forward RC structure, the whole control system is modified to include the RC controller $G_{rc2}(z)$ as shown in Figure 2.11 [66].

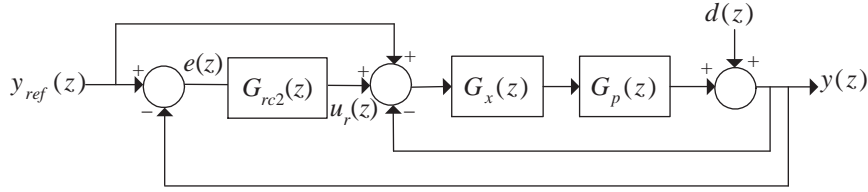


Figure 2.11: RC structure adjusting the command to a feedback control system but modified to include feed-forward command signal.

Plug-in RC structure

The most commonly used plug-in repetitive control system is shown in Figure 2.12 [66]. Plug-in RC control structure is very easy to plug into a stable, already operating closed-loop control system without any modifications. It can be seen in Figure 2.12 where RC represented by $G_{rc3}(z)$ can be plugged in/out at any time. It can also be noticed that feed-forward and plug-in RC structures produce same result, if the signal input to the conventional feedback controller $G_x(z)$ is examined.

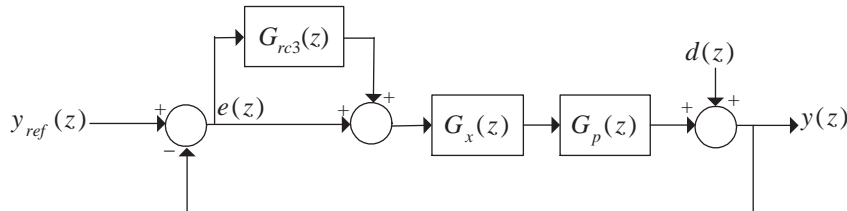


Figure 2.12: Plug-in RC control System.

2.3.3 Transfer Function of Plug-In RC Control System

From Figure 2.6 the transfer functions from $y_{ref}(z)$ and $d(z)$ to $y(z)$ in the overall closed-loop system, are:

$$\begin{aligned} \frac{y(z)}{y_{ref}(z)} &= \frac{(1 + G_{rc}(z))G_x(z)G_p(z)}{1 + (1 + G_{rc}(z))G_x(z)G_p(z)} \\ &= \frac{\left\{1 - z^{-N_o} \left(Q(z)(1 - k_r G_c(z)) \right)\right\} H(z)}{1 - z^{-N_o} \left\{ Q(z)(1 - k_r G_c(z)H(z)) \right\}} \end{aligned} \quad (2.5)$$

$$\frac{y(z)}{d(z)} = \frac{(1 + G_x(z)G_p(z))^{-1} (1 - z^{-N_o} Q(z))}{1 - z^{-N_o} Q(z)(1 - k_r G_c(z)H(z))} \quad (2.6)$$

where

$$H(z) = \frac{G_x(z)G_p(z)}{1 + G_x(z)G_p(z)} = \frac{z^{-d} B^+(z^{-1}) B^-(z^{-1})}{A(z^{-1})} \quad (2.7)$$

where $d \in \mathbb{R}$ is the known delay steps of the system, $B^+(z^{-1})$ and $B^-(z^{-1})$ are the cancelable and un-cancelable parts of the numerator, and $A(z^{-1}) = 0$ is the system characteristic equation. In order to achieve zero-phase compensation, the compensating filter $G_c(z)$ needs to be the exact inverse of (2.7) but practically it is impossible to achieve the exact inverse of the system due to parameter uncertainties and unmodelled dynamics of the system. Thus $G_c(z)$ can be chosen as [40, 43, 55]:

$$G_c(z) = \frac{z^d A(z^{-1}) B^-(z^{-1})}{B^+(z^{-1}) b} \quad (2.8)$$

where $b \geq \| B^{-1}(z^{-1}) \|^2$. The delay steps d can be determined by experiments in practical applications.

2.3.4 Stability of RC System

From (2.5) – (2.8) it is clear that the closed-loop system of Figure 2.6 is stable if the following two conditions are fulfilled [41, 45, 67, 72].

- The closed-loop system without the RC controller ($G_{rc}(z)$) is stable, *i.e.* the poles of $H(z)$ are inside the unit circle, where

$$H(z) = \frac{G_x(z)G_p(z)}{1 + G_x(z)G_p(z)} \quad (2.9)$$

If the roots of $1 + G_x(z)G_p(z) = 0$ lie inside the unit circle, it ensures that the closed-loop system containing plant and conventional feedback controller is stable.

- The roots of $1 - z^{-N_o} Q(z)(1 - k_r G_c(z)H(z)) = 0$ also reside in the stable region *i.e.* inside unit circle, then

$$|Q(z)| |1 - k_r G_c(z)H(z)| < 1, \forall z = e^{j\omega} \quad (2.10)$$

where $|Q(z)|$ represents the magnitude of low-pass filter $Q(z)$ and $\omega \in [0, \pi]$.

2.4 REPETITIVE CONTROL UNDER VARYING FREQUENCY CONDITIONS

Repetitive control requires that the frequency of the signal to be tracked/rejected (reference signal) is well known and invariant. However, in practical applications it is not always possible to keep the frequency of the reference signal constant. In electrical power systems, loads are continually turning on and off which causes continuous perturbations to the power system. The difference between the instantaneous generation and loading plus losses causes either a speeding up or slowing down of the synchronous machine generators, manifesting itself as a frequency variation. The balance between generated and consumed power is stored or extracted from the kinetic energy of the rotating machine. Frequency keeping generators detect this frequency change and adjust their real power output to correct this frequency deviation. The size of the frequency variation is a function of the system inertia and hence size of the system. Small island networks (such as New Zealand) exhibit a relatively large variation in system frequency and power electronic inverters must be able to operate correctly and meet performance criteria (such as harmonic levels) in this environment.

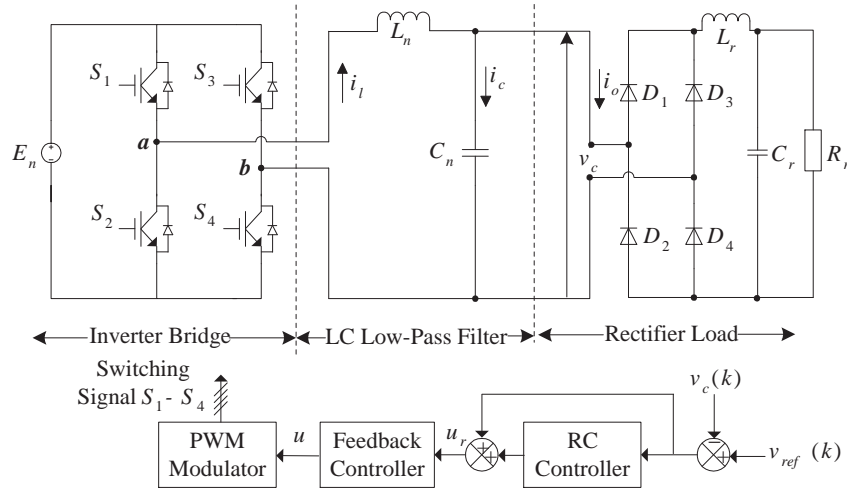
Grid connected inverters inject the generated dc energy into the ac utility grid. The ac electric energy from the inverter has to be compatible with the energy within the ac utility system at the point where the inverter is connected to the utility system. Thus, the inverter must be capable of tracking the varying frequency signal of the grid.

To investigate the performance of repetitive control under varying frequency conditions, an RC controlled single-phase inverter and a three-phase rectifier have been simulated.

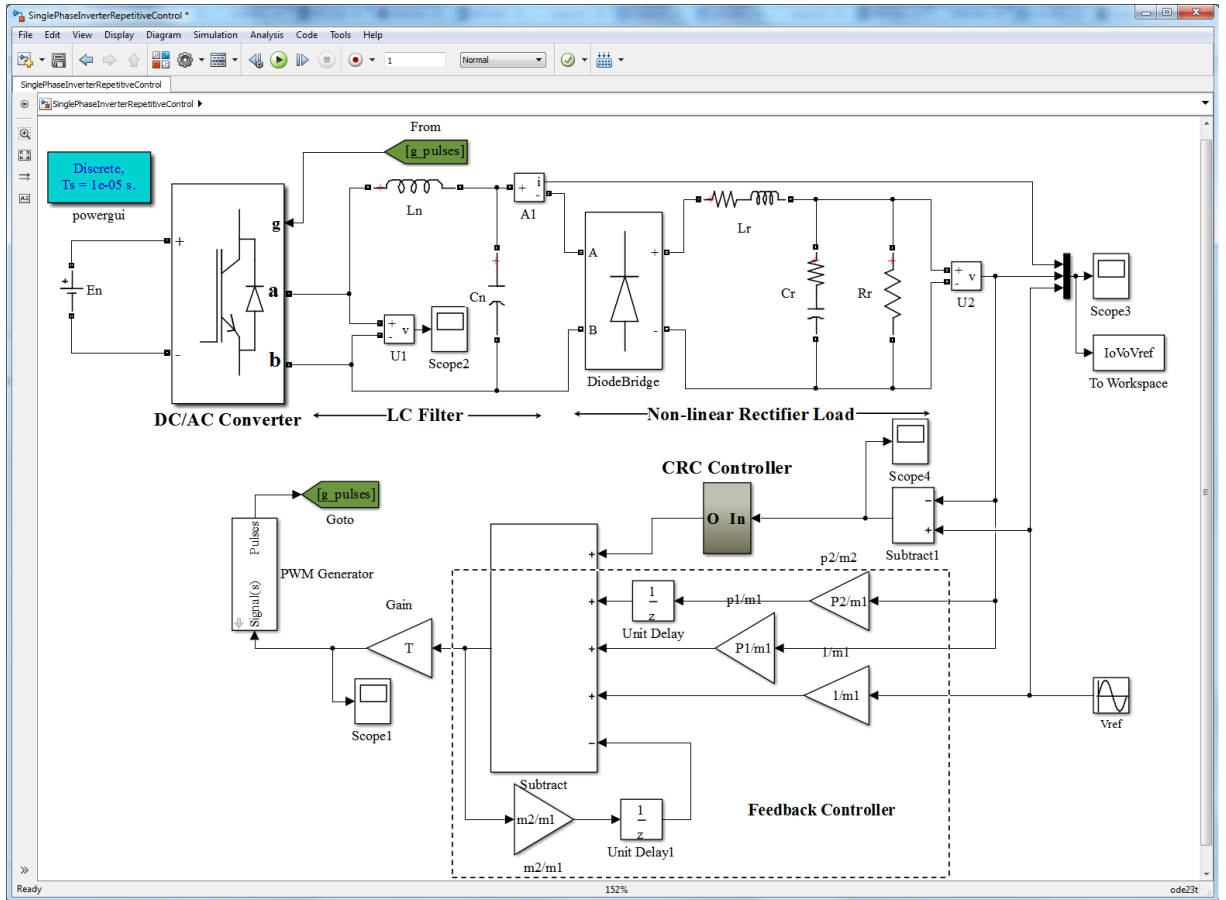
2.4.1 RC Controlled Single-Phase Inverter

Inverters, also known as dc-ac converters, convert dc power to ac power at desired output voltage or current and frequency. A stand-alone, single-phase PWM inverter, connected to a non-linear load is shown in Figure 2.13. In the block diagram (Figure 2.13a), E_n denotes the nominal value of the dc bus voltage; L_n and C_n denote nominal values of filter inductor and capacitor; L_r , C_r and R_r denote rectifier load parameters (inductor, capacitor and resistor); v_c and i_o represent load voltage and current; $v_{ref}(k)$ denotes the reference signal in the k^{th} sampling instant. For stand-alone inverters the reference signal is separately provided by an ac source or it can be internally created by microprocessor by specifying the frequency and amplitude of the sine wave, whereas in case of grid connected inverters, output of the inverter is also connected to the utility grid and the grid voltage acts as a reference signal which is fed to controller. The inverter in Figure 2.13 is using a feedback controller (FC) and RC controller to maintain the required ac output voltage. Compared with the FC, RC shows slow dynamic response due to its long delay time between input and output. In order to achieve high performance control, RC controller is usually plugged into the FC controlled systems. The main purpose of FC here is to stabilize the plant. The FC controller offers fast transient response and robustness whereas the RC controller ensures high tracking accuracy. The objective of the RC controller is to track a reference periodic signal in the presence of non-linear loads and parameter uncertainties. Due to non-linear loads and parameter uncertainties, the output voltage of the inverter often suffers from periodic tracking errors, which are major sources of total harmonic distortion.

Figure 2.13b shows the Simulink model of a single-phase dc/ac converter. The dc bus voltage (E_n) is set to 350 V and reference signal to be tracked is a varying frequency signal ($v_{ref} = 170\sin(2\pi ft)$) where $f = 49 \sim 51$ Hz. $L_n = 5$ mH, $C_n = 3$ μ F, $L_r = 1$ mH, $C_r = 600$ μ F, $R_r = 10$ Ω , sampling/switching frequency $f_s = f_{sw} = 5$ kHz and sampling period $T_s = 1/f_s$ are used. The Simulink model has slightly different variable names due to duplicate elements and constraints on naming elements in Simulink. Feedback controller parameters have been calculated



(a) Block diagram of RC controlled single-phase PWM inverter.



(b) Simulink model of RC controlled three-phase rectifier.

Figure 2.13: Control details of three-phase PWM rectifier.

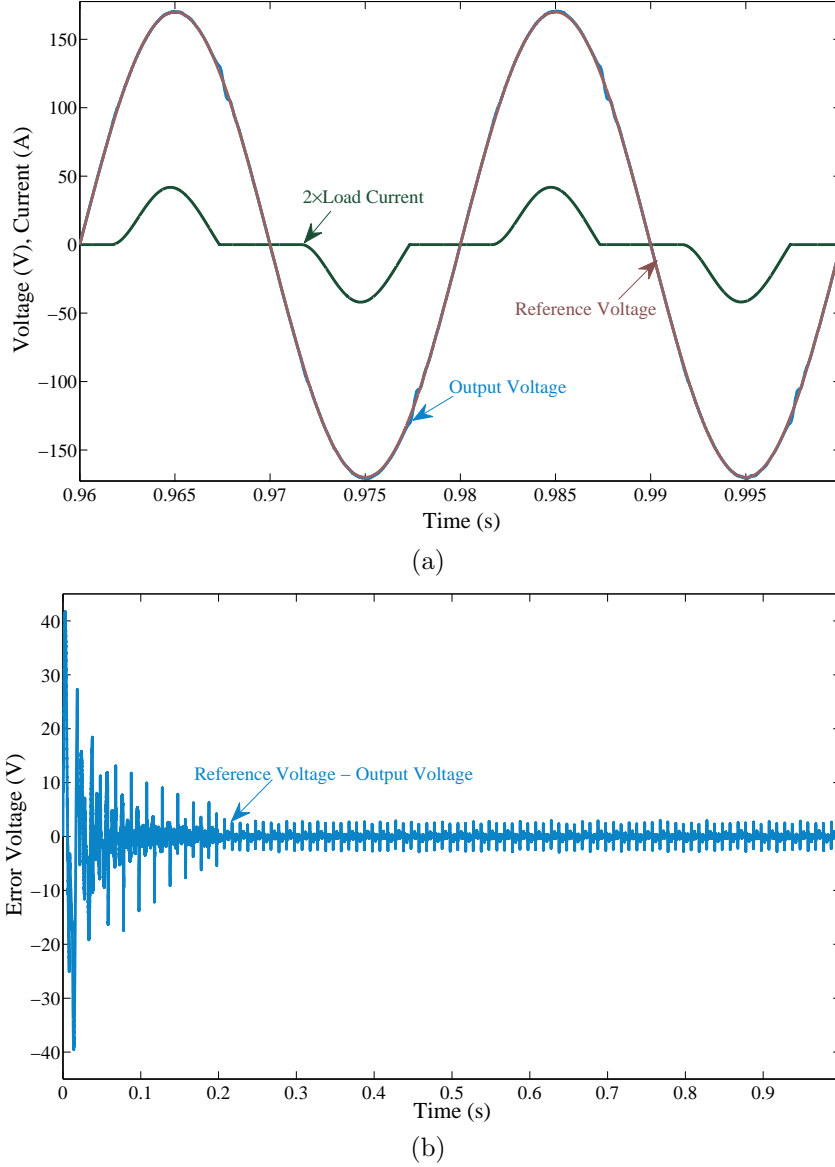


Figure 2.14: RC and deadbeat controlled single-phase inverter when samples per period is integer
(a) Steady-state response of converter voltage (b) Transient response of voltage tracking error.

based on inverter system and component values. The design procedure of FC controller is not included in this research work. A deadbeat controller has been used as FC in this research.

Figure 2.14 shows the response of RC controlled inverter when the frequency of the reference signal is 50 Hz and $N_o = 100$ (*i.e.* N_o is integer). It is clear that the output voltage is tracking the reference signal very well and the steady-state voltage tracking error (peak) is less than 3 V (*i.e.* 1.76 %).

Figure 2.15 shows the response of an RC controlled inverter when the frequency of the reference signal is 50.2 Hz ($N_o = 99.6$) *i.e.* N_o is non-integer. A CRC controller cannot operate for fractional values of N_o . Therefore, when such cases occur the value of N_o is usually rounded off to the nearest integer. It can be seen from Figure 2.15, that the output voltage is still tracking the reference signal but the steady-state voltage tracking error (peak) is now greater than 10 V (5.9 %). The error has been significantly increased for a small deviation in the reference signal frequency. Therefore, the performance of RC control under varying frequency environment may become unacceptable.

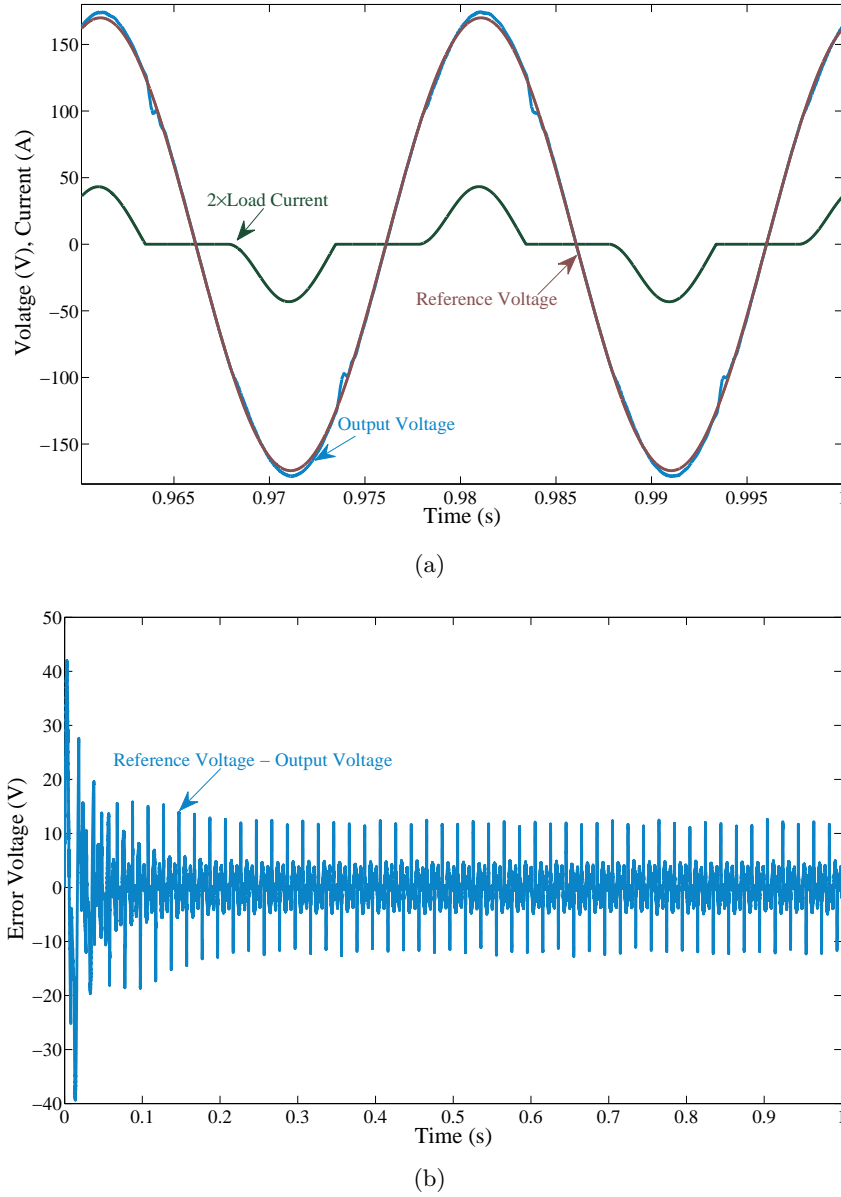
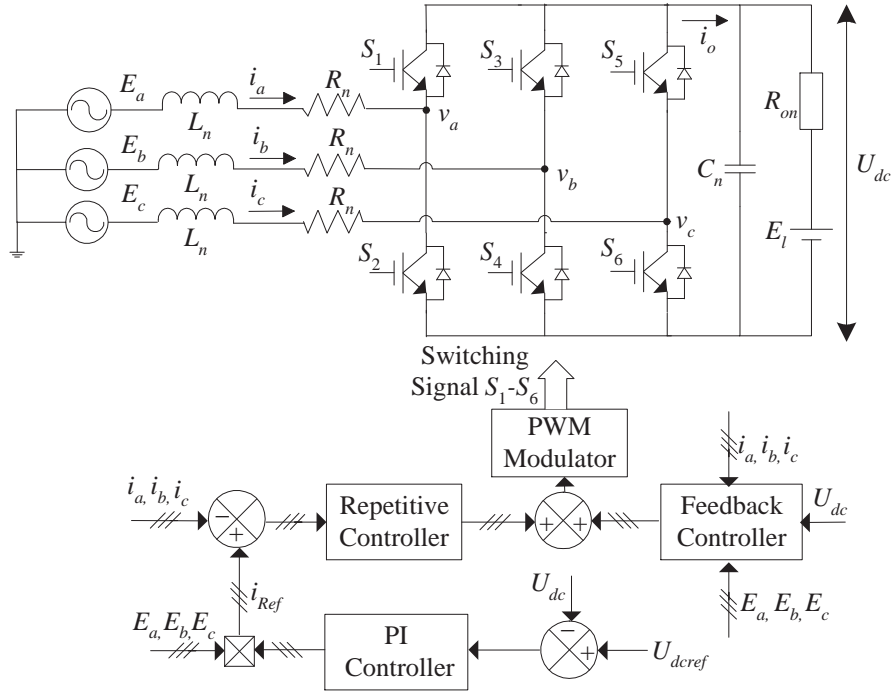


Figure 2.15: RC and deadbeat controlled single-phase inverter when samples per period is non-integer (a) Steady-state response of converter voltage (b) Transient response of tracking error.

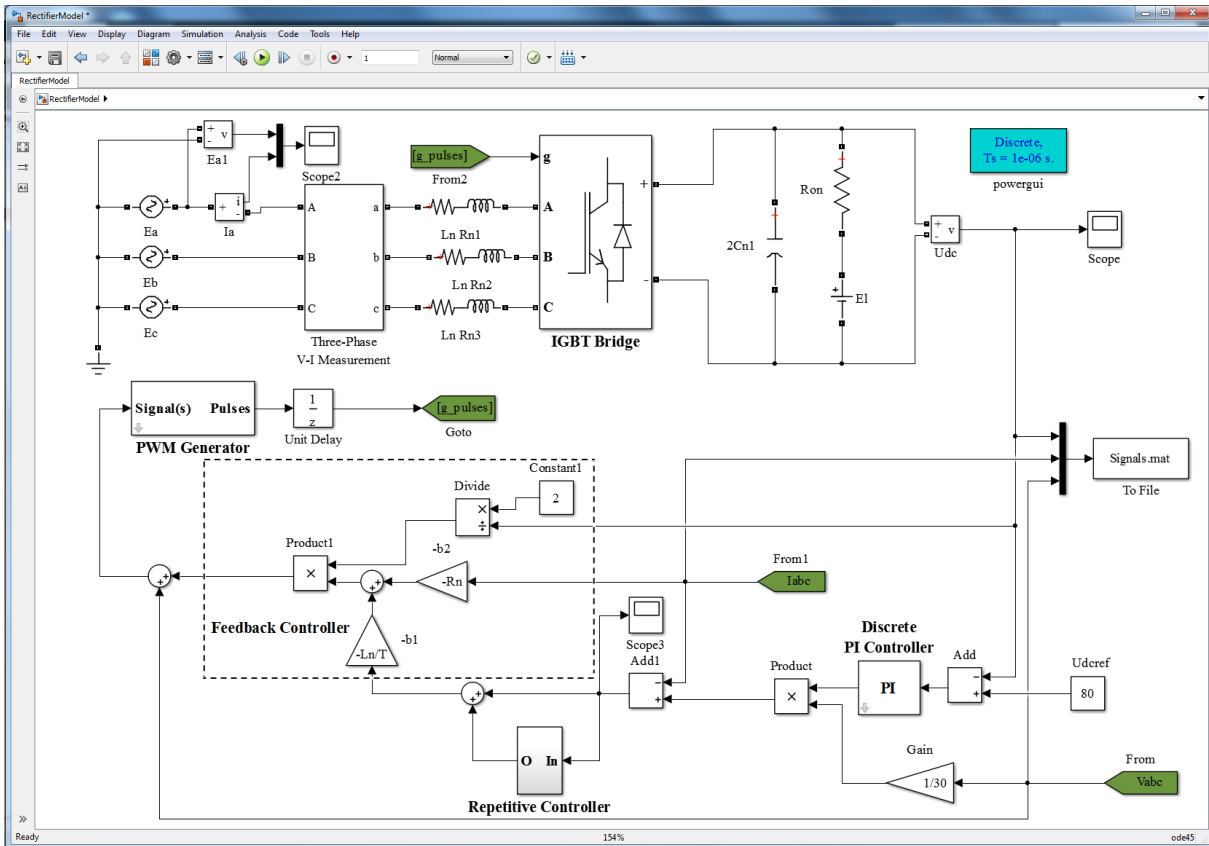
2.4.2 RC Controlled Three-Phase PWM Rectifier

Rectifiers convert ac power to dc power and they are widely used in many applications including battery charging, dc motor drives and power supplies for microelectronics. PWM converters use controlled semi-conductor devices, such as Insulated Gate Bipolar Transistors (IGBTs), Metal Oxide Semi-conductor Field Effect Transistors (MOSFETs) and Gate Turn Off Thyristors (GTOs), and actively change the waveform of the input current.

Figure 2.16 represents a block diagram and a Simulink model of an RC controlled three-phase PWM rectifier. In block diagram E_a , E_b and E_c represent the three-phase ac source voltages; i_a , i_b and i_c are the feeding in/out phase currents; U_{dc} is the output dc bus voltage; $v_a = u_a U_{dc}/2$, $v_b = u_b U_{dc}/2$ and $v_c = u_c U_{dc}/2$ are the PWM modulated voltages with u_a , u_b , u_c being the normalized control outputs of the controller; L_n , R_n , C_n are the nominal values of ac-side inductor, ac-side resistance and the dc bus capacitor respectively; R_{on} is the load resistance and E_l is the emf of the load.

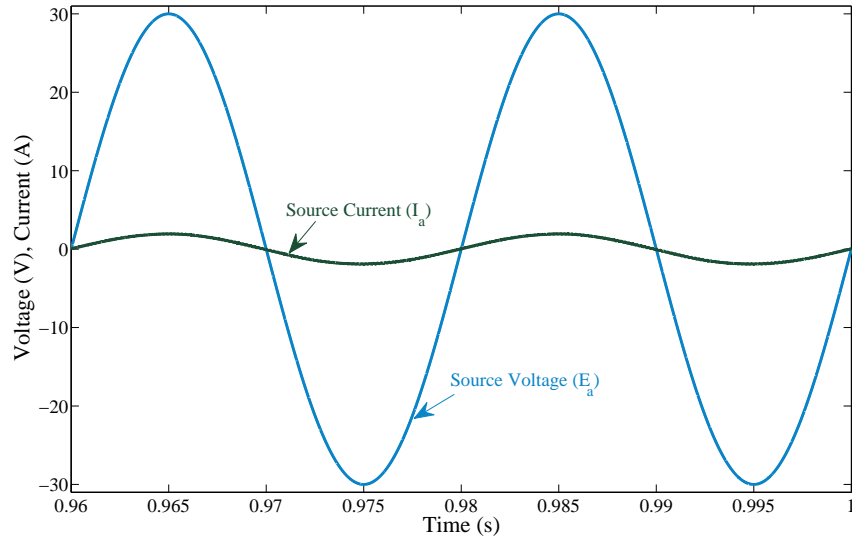


(a) Block diagram of RC controlled three-phase PWM rectifier.

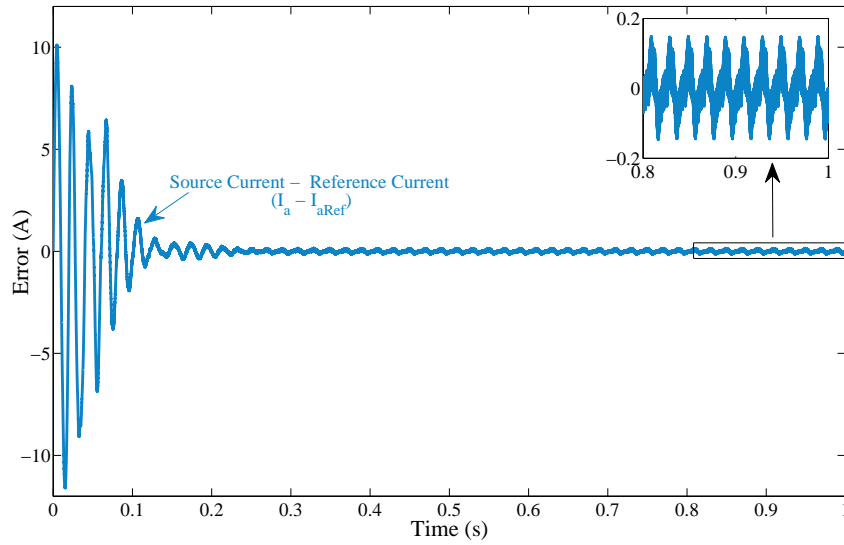


(b) Simulink model of an RC controlled three-phase rectifier.

Figure 2.16: Control details of three-phase PWM rectifier.

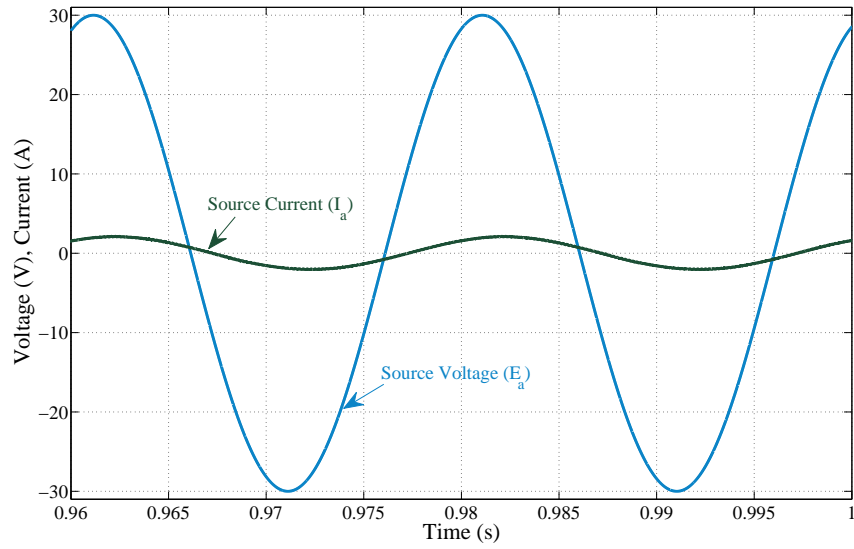


(a)

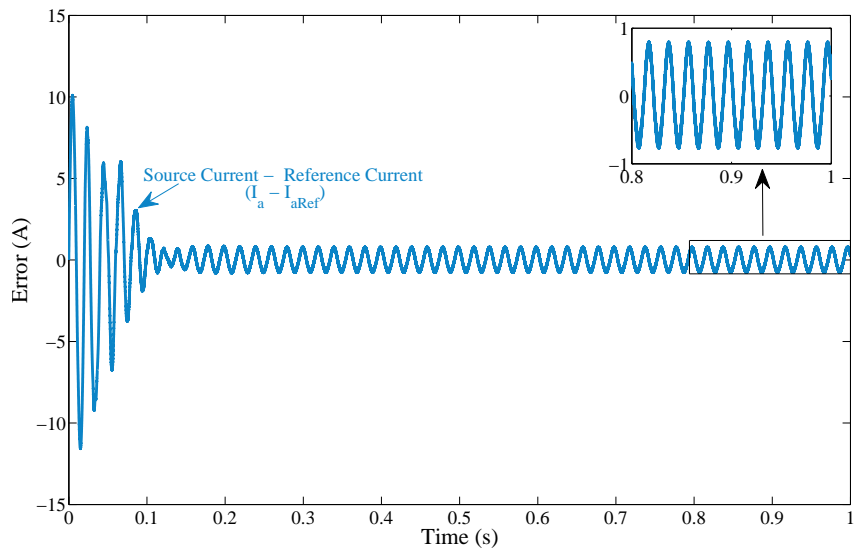


(b)

Figure 2.17: RC controlled three-phase rectifier when samples per period is integer (a) Steady-state response of ac-side voltage and current (b) Transient response of current tracking error.



(a)



(b)

Figure 2.18: RC controlled three-phase rectifier when samples per period is non-integer (a) Steady-state response of ac-side current (b) Transient response of current tracking error.

The three-phase rectifier is required to maintain a constant dc output voltage (U_{dc}) while drawing a sinusoidal current from the ac source in the presence of disturbances and parameter uncertainties. To achieve a constant dc bus voltage, a PI controller is employed whereas the current controller is composed of RC controller and a conventional feedback controller. In case of grid connected converters, the grid acts as a three-phase ac source and the frequency of the grid is not constant. The Simulink model has slightly different variable names due to duplicate elements and Simulink constraints on naming elements.

The three-phase PWM rectifier simulated in Simulink MATLAB has following system parameter values: $E_{j(j=a,b,c)} = 30\sin(2\pi ft + \theta)$, where f is the frequency of the input signal and $\theta = \{0^\circ, 120^\circ, 240^\circ\}$, $L_n = 15$ mH, $R_n = 0.5 \Omega$, $C_n = 4400 \mu\text{F}$, $R_{on} = 100 \Omega$, $E_l = 0$ V, sampling and switching frequency $f_s = f_{sw} = 5$ kHz and reference dc bus voltage $U_{dcref} = 80$ V.

The conventional feedback and plug-in repetitive controller have been used together to achieve the advantages of both feedback controller and plug-in repetitive controller. More details about using two controllers simultaneously are given in Section 6.3.1. The conventional FC controller offers fast response and good robustness whereas the RC controller presents zero steady-state error with slow dynamic response [45].

Figure 2.17 shows the response of RC controlled rectifier with grid frequency of 50 Hz (*i.e.* $N_o = 5 \text{ k}/50 = 100$) in steady-state, where power factor is unity and steady-state current tracking error (peak) is less than 0.2 A. It shows that the RC controller is working well when the value of N_o (samples per period) is integer.

To investigate the behaviour of the repetitive controlled converter in the presence of grid frequency variations the frequency (f) of the three-phase ac source was changed from 50 Hz to 50.2 Hz. The sampling frequency was unchanged *i.e.* 5 kHz and thus the number of samples per period ($N_o = f_s/f$) became non-integer ($N_o = 99.6$). Since the CRC scheme is unable to work with non-integer value of N_o so N_o is rounded off to the nearest integer value that is $N_o = 100$. Figure 2.18 shows the effect of grid frequency variation on tracking accuracy and input ac-side current; steady-state tracking error has increased up to 1 A and phase angle between input voltage and current is fluctuating leading to the power flow oscillations.

All the simulation results show that uncontrolled grid frequency variations may lead to power-flow oscillation between the converter and the grid. The peak-to-peak current tracking error significantly increases due to the grid frequency variation when the samples per period become non-integer and are rounded off to the nearest integer to work with CRC schemes. In case of grid connected converters the frequency of the grid is an uncontrolled parameter and based on simulations given in this section it has been concluded that the performance of RC control degrades drastically when the samples per period become non-integer and the sampling frequency is fixed. Thus the preliminary work showed that new and advanced repetitive control strategies need to be developed to deal with fractional period periodic signals.

2.5 CONCLUSION

This Chapter gives an overview of RC controllers and analyzes the performance of the digital repetitive control systems subjected to time varying period reference signals. Under such circumstances and fixed sampling rate, the number of samples per period ($N_o = T/T_s$) may become non-integer and CRC approach rounds off the N_o to its nearest integer value. Two application examples (single-phase inverter and three-phase rectifier) have been used to show the effect of a variable frequency reference signal on the performance of the CRC control scheme. The examples show that the CRC approach does not perform well under varying frequency conditions and steady-state error is high. Advanced repetitive control strategies are needed to deal with the issue of a variable frequency reference signal leading to non-integer number of samples per period.

Chapter 3

HARDWARE IMPLEMENTATION

3.1 INTRODUCTION

The objective of this Chapter is to present the design and development of the power and control electronics for single-phase inverter and three-phase rectifier test rigs used in experimental investigations of Chapter 4, 5 and 6. In particular a description of LC low-pass filter stage, signal (voltage and current) conditioning circuit boards, single-phase and three-phase PWM control boards design and details of used equipment is given in this Chapter. A general test rig for three-phase converter is designed which is adaptable for single-phase converters as well.

3.2 EXPERIMENTAL SETUP DESCRIPTION

A test rig is designed and built for experimental verifications. MATLAB/Simulink, dSPACE control kit, SEMIKRON converter system, Chroma programmable dc power supply, electronic load, PWM control board, signal conditioning circuit boards and various metering devices are employed to construct the hardware-in-loop test rig as shown in Figure 3.1.

Initially, the test rig is developed for a three-phase PWM converter circuit. The voltage and current conditioning circuit boards are also designed for three-phase measurements. However, they are also used for single-phase measurements. The PWM control boards for the three-phase and single-phase converters are designed separately. The three-phase and single-phase PWM control boards design is explained in greater detail in section 3.3.2.

The test rig development for three phase inverter supplying a resistive load is explained, in detail, in this section.

3.3 HARDWARE DESIGN

The experimental setup shown in Figure 3.1 has two stages: the power stage and control stage. The power stage consists of a Chroma dc voltage source, a SEMIKRON converter system, a second order LC filter and a load supplied by Chroma ac/dc electronic load. The control stage consists of signal conditioning circuits, PWM control circuit, MATLAB/Simulink, dSPACE (1103) hardware and software tools.

In this Section, design of the power and control stage for a three-phase dc/ac converter system connected to a resistive load is discussed. In the block diagram v_{ab} , v_{bc} , and v_{ca} denote PWM modulated voltages; i_A , i_B , i_C denote inductor currents; v_{12} , v_{23} , and v_{31} denote the output line-to-line voltages; E_n , L_n , C_n and R_n denote nominal values of dc bus voltage and components (filter inductor, filter capacitor and load resistance).

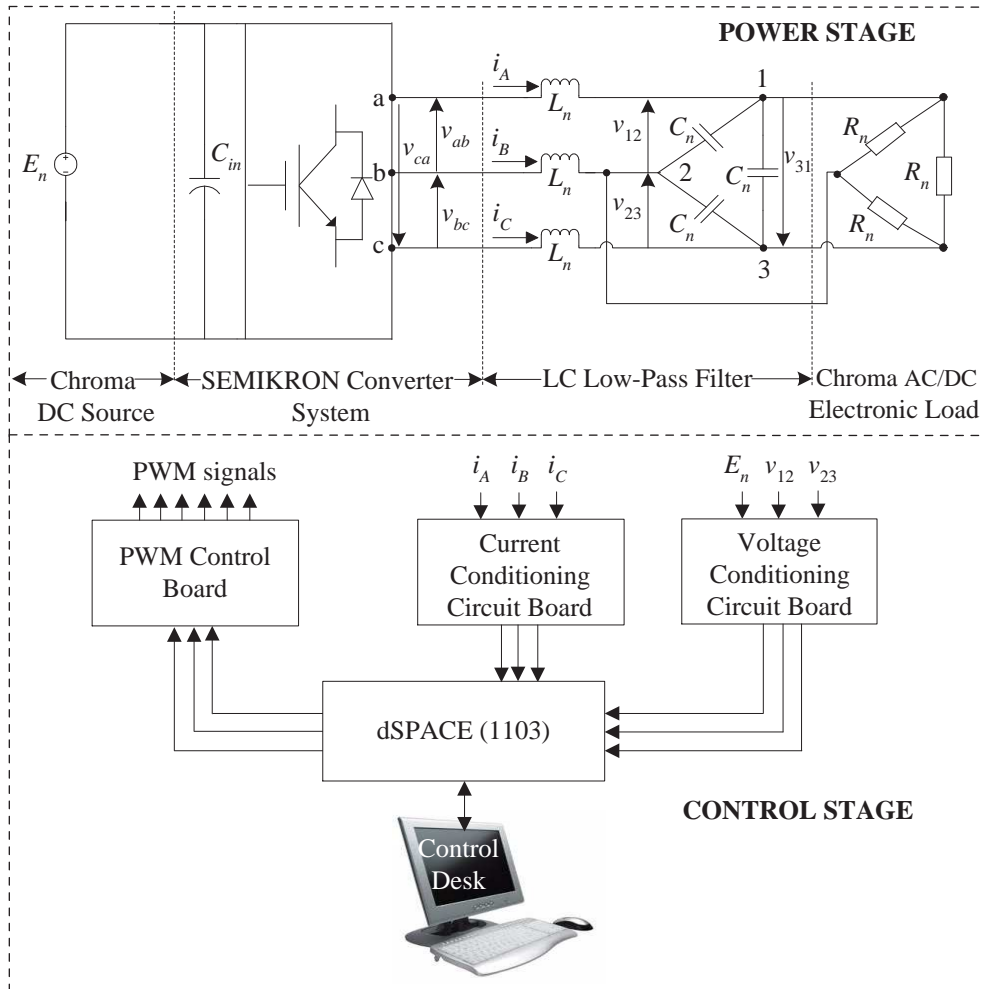


Figure 3.1: Block diagram of the overall experimental setup.

The three-phase PWM inverter specifications are given in Table 3.1.

Table 3.1: Specifications of the three-phase inverter.

Output line-to-line voltages	$v_{12}, v_{23}, v_{31} = 110 \text{ V (rms)}, 50 \text{ Hz}$
Inductor currents	$i_A, i_B, i_C \leq 10 \text{ A (peak)}$
Total rated output power	$P = 2 \text{ kW}$
Filter inductor	$L_n = 5 \text{ mH}$
Sampling and switching frequency	$f_s = 10 \text{ kHz}$

3.3.1 Power Stage

The dc bus voltage (E_n), supplied by a Chroma programmable dc source, is determined by the required output ac voltage and the modulation index (D_i) as shown in (3.1) [73]:

$$E_n = \frac{2\sqrt{2}v_{12}}{\sqrt{3}D_i}, \quad (D_i \leq 1) \quad (3.1)$$

D_i is defined as:

$$D_i = \frac{v_{control}}{v_{triangle}} \quad (3.2)$$

The PWM pulses, output of the control stage in Figure 3.1, are generated by comparing a reference modulating signal $v_{control}$ to a triangular carrier waveform $v_{triangle}$.

Programmable Chroma dc source

The programmable Chroma (62150H-600S) dc source (shown in Figure 3.2) is employed in all tests to supply the dc voltage E_n . The Chroma dc source emulates a distributed generator (*e.g* solar array). This programmable dc source is capable of supplying a maximum power of 15 kW with a voltage up to 600 V and current up to 25 A.

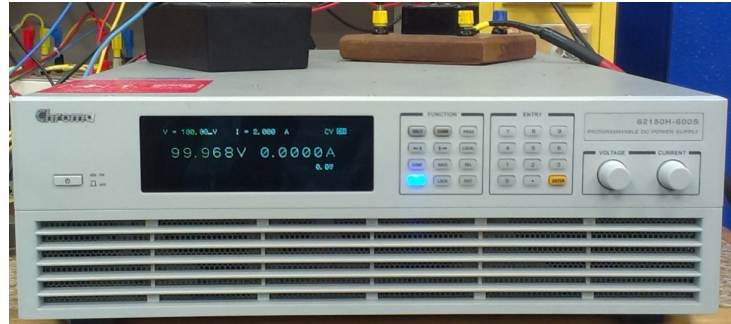


Figure 3.2: A programmable Chroma (62150H-600S) dc source.

Its main features include fast transient response solar array simulation, simulation of multiple solar cell material I-V characteristics, shadowed I-V curve output simulation, very low leakage current ($< 3 \text{ mA}$), precise voltage and current measurements, Graphical User Interface (GUI) and data recording [74]. Thus this source is simulated as a practical distributed generator in experiments. The voltage measurement can be configured in two modes: a range between 0 and 120 V or between 0 and 600 V, having an accuracy of $0.05\% + 0.05\%$ full scale, *i.e.* for low voltages, it provides more accurate measurements if the selected measurement range is between 0 and 120 V. Similarly, the current measurement offers two modes: a range between 0 and 10 A or

between 0 and 25 A, having an accuracy of $0.1\% + 0.1\%$ full scale. The programmable Chroma dc power supply can be operated from the front panel keypad or from the remote controller via USB / RS232 / RS485 / APG (standard), GPIB and Ethernet. Only the front panel keyboard operation is utilized throughout our experimental investigations.

This source offers front panel programming accuracy of 0.1% of V_{max} in voltage and 0.3% of I_{max} in current, and a programming resolution of 10 mV and 1 mA. The output voltage ripple is 1500 mV peak-to-peak and 650 mV rms, while the output current ripple is 450 mA rms. The transient response time is 1ms to $\pm 0.75\%$ of steady-state output for a 50% to 100% or 100% to 50% load change ($1 \text{ A} / \mu\text{s}$) [74].

SEMIKRON converter system

The input capacitor C_{in} in Figure 3.1 is the dc link filtering capacitor and it is required to hold the dc bus voltage constant. SEMIKRON converter system already contains two electrolytic capacitors connected in series, their individual value is $2200 \mu\text{F}/400 \text{ V}$. The equivalent value of the dc bus capacitor is $1100 \mu\text{F}/800 \text{ V}$. Theoretically, this value is to be determined by the desired filtering quality (capacitance/voltage). The size of electrolytic capacitor among many other factors also depends upon the rms value of allowed capacitor current. This chosen capacitor size fulfills almost all applications in the range of power addressed by the SEMIKRON converter system.

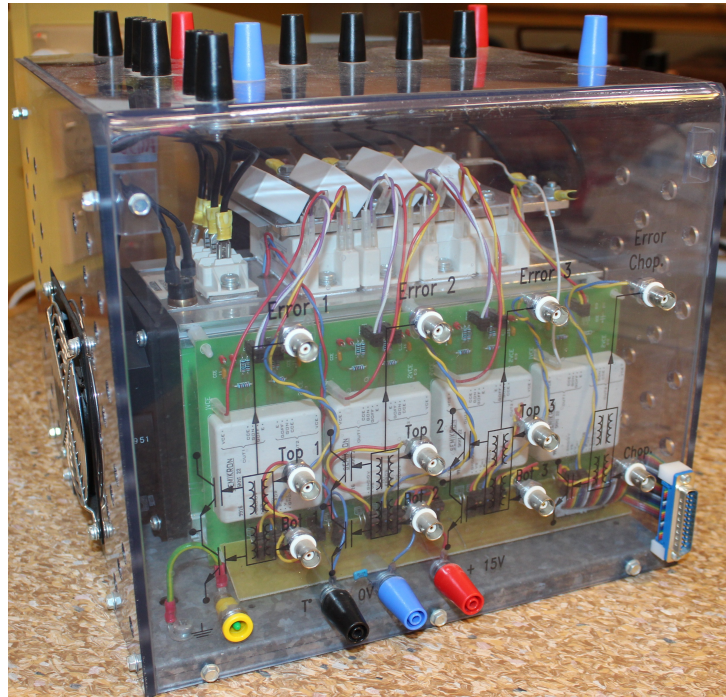


Figure 3.3: A SEMIKRON converter system.

Figure 3.3 shows a SEMIKRON converter system. It contains six IGBT switches connected in full bridge configuration, gate driver unit, three-phase diode bridge rectifier, filtering capacitors and thermal protection devices as shown in Figure 3.4.

The PWM signals from the control stage (Figure 3.1) are supplied to the gate driver units of the SEMIKRON unit. A gate drive circuit amplifies the logic level control signals and delivers high peak current for the switching of the IGBT module. Table 3.2 lists the parameters of the SEMIKRON converter system which are very important to know before designing a converter using SEMIKRON system.

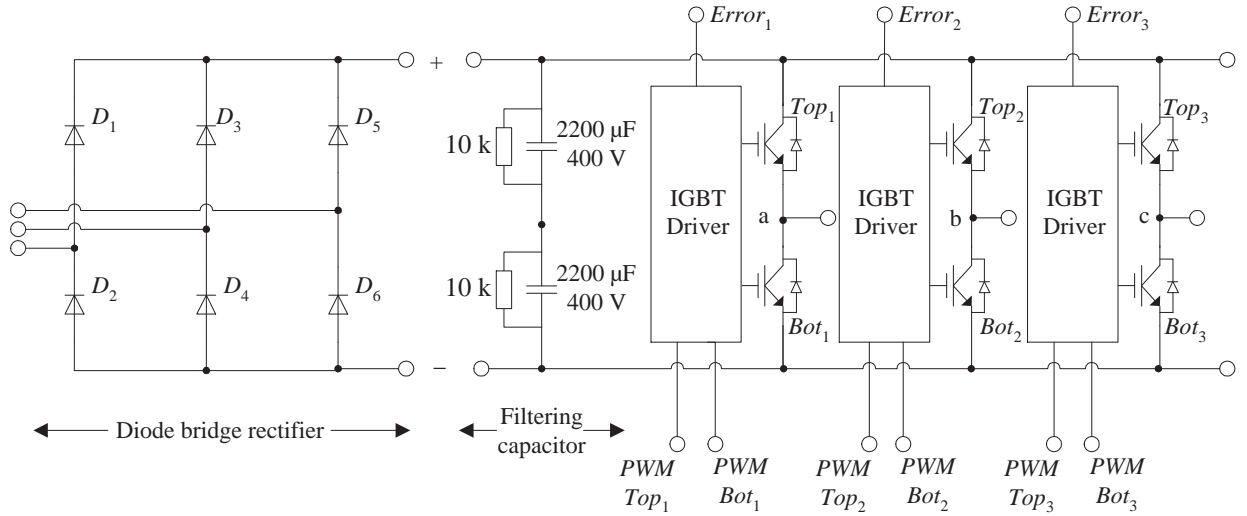


Figure 3.4: SEMIKRON converter system overview.

The three error voltages ($Error_1$, $Error_2$, $Error_3$) from the converter are negative logic *i.e.* error voltage is 15 V in case of no error and it goes down to zero if error occurs in the system. These error voltages have been continuously monitored using a voltage conditioning circuit board (Section 3.3.2) for protection and safety of the system.

Table 3.2: Parameters of SEMIKRON converter system.

Parameter	Voltage level	Max. current level	Parameter	Value
IGBT inverter input	600 Vdc	30 A	Driver power supply	15 V
IGBT inverter Output	400 Vac / 600 Vdc	30 A	Max. switching frequency	50 kHz
Rectifier input	230/400V	30 A	Top-bottom interlock	3 μ s
Rectifier output	600 Vdc	30 A	Operating temperature	-40...+85°C
PWM input of inverter	C-MOS logic 0/15 V	1 A	Temperature sensor output	5 V
Error output of inverter	0/15 V	1 A		

The output of the inverter is a high frequency (equal to switching frequency) PWM waveform. An LC low-pass filter follows the SEMIKRON converter system which removes high frequency content. The filter is designed based on the inverter specifications given in Table. 3.1.

LC low-pass filter

The second-order LC filter shown in Figure 3.5 filtered out undesired switching frequency components from the converter output voltage.

The delta connected capacitors are transformed to star connected ones, for ease of analysis as shown in Figure 3.6.

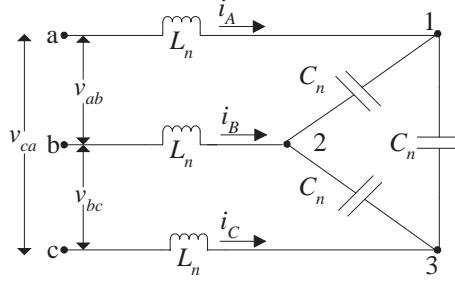


Figure 3.5: Second order low-pass LC filter.

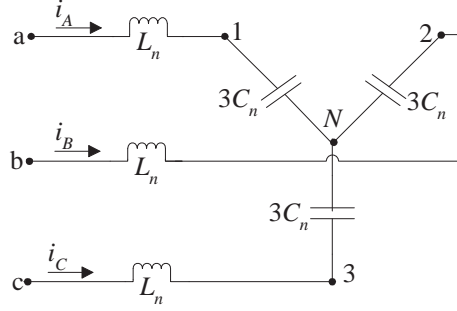


Figure 3.6: Equivalent LC filter.

The system in Figure 3.6 can be decoupled into three identical single-phase systems as given in Figure 3.7.

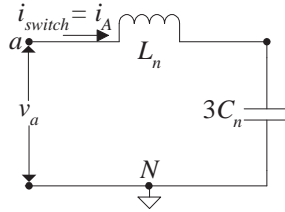


Figure 3.7: Equivalent LC filter per phase.

Bandwidth of LC filter: In Figure 3.7, the input v_a is the output of the converter which is a PWM signal containing fundamental frequency component ($f = 50\text{Hz}$) and harmonics. The LC filter filters out the high frequency component and gives a low frequency signal at the output ($f = 50\text{Hz}$ in this case). The Band-Width (BW) of the LC filter shown in Figure 3.7 is reasonably greater than the desired output frequency f and less than the sampling frequency f_s so that it could effectively filter out the undesired frequency content. The bandwidth of low-pass filter in Figure 3.7 is given by:

$$BW = \frac{1}{2\pi\sqrt{L_n(3C_n)}} \quad (3.3)$$

$$BW = [5f, 8f] \ll f_s \quad (3.4)$$

Equations (3.3) and (3.4) gives $L_n C_n \in [5.28e^{-8}, 1.35e^{-7}]$. A few 5 mH/20 A inductors were already available in Power Electronics Laboratory and they are used to construct the LC filter, thus a range of capacitor values $C_n \in [11, 27] \mu\text{F}$ is obtained. The LC filter is optimized to select a value of filter capacitor from the available range.

Optimization of LC filter

For optimization of the LC filter, the current through the IGBT switches is selected to be a measure of the performance of the filter. The inductor current i_A in Figure 3.7 is calculated as:

$$i_A = \frac{v_A}{Z_l + Z_c} \quad (3.5)$$

where, Z_l and Z_c represent the inductor and capacitor impedances at the reference frequency *i.e.* 50 Hz. Eq. (3.4) provided a range of $L_n C_n$ values. As L_n is fixed to 5 mH in our case, a range of C_n values is obtained. Table 3.3 shows the fundamental frequency current demand from the switches under different capacitor values when L_n is fixed to 5 mH.

Table 3.3: Current demand from IGBT switches for various LC filter parameters.

L_n (mH)	C_n (μ F)	$i_A = i_{switch}$ (A)
5	11	1.64
5	20	3.02
5	27	4.12

Table 3.3 indicates that higher capacitance resulted in more current demand from the L_n and the switches, and more reactive power flows into the capacitor. Thus, a smaller and standard value of filter capacitor $C_n = 20 \mu$ F is selected.

Chroma ac/dc electronic load

The Chroma (63802) programmable ac/dc electronic load shown in Figure 3.8 is used to load the converter. This programmable ac/dc source has a power rating of 18 kW, voltage range 50 V - 350 V rms (500 V peak) and a current range 0 - 18 A rms (54 A peak). It is capable of operating in constant resistance, constant voltage, constant current, constant power and rectifier RLC load mode. The constant resistance and rectifier RLC mode have been used in our case.



Figure 3.8: Programmable Chroma ac/dc electronic load.

In all four modes of operation of the electronic load, various parameters (like load resistance, maximum allowed current) can be set and measured very accurately. The current accuracy is 0.1% of set value + 0.2% of range. The resistance range is $2.77 \Omega \sim 2.5 k\Omega$ with an accuracy of 0.5% of set value + 0.5% of range and a resolution of $20 \mu\Omega$. For ac quantities, the frequency range of the fundamental component is between 45 Hz and 440 Hz. In case of rectifier RLC mode the range for inductance capacitance and resistance is $0 \sim 9999 \mu$ H and $100 \sim 9999 \mu$ F and $2.77 \sim 9999.99 \Omega$ respectively [75]. The Chroma load also provides internal self diagnosis routines and protection against over-power, over-current, over-voltage and over-temperature.

The Chroma source also includes built-in 16-bit precision measurement circuits to measure the transient and steady-state responses for true rms voltage and current; true active (P), reactive

(Q) and apparent power (S); crest factor, power factor, THD and peak current. All these discrete measurements are continuously displayed on the screen. In addition to discrete measurements, two analog outputs, one for voltage and one for current, can be monitored via an external oscilloscope.

According to Table 3.1, the inductor current is limited to 10 A (peak). The load affects the current flowing through the inductor so a limit on load resistance is calculated so that the converter can perform well according to the specification given in the Table 3.1.

A delta connected resistive load (R_n) attached to the output of the LC filter is shown in Fig 3.9. The linear resistive load is only considered here to simplify the design procedure. Practically the experiments are performed with more realistic non-linear rectifier loads as well. Since the maximum allowed current through the SEMIKRON IGBT switches is 30 A [Table 3.2] so the load and LC filter should ensure that the current never exceeds the current rating of the SEMIKRON converter. However, in our case, for safety reasons, the three-phase inverter is designed so that the maximum current through IGBT switches does not exceed 10 A. *i.e.* $i_A \leq 10$, $\forall R_n$.

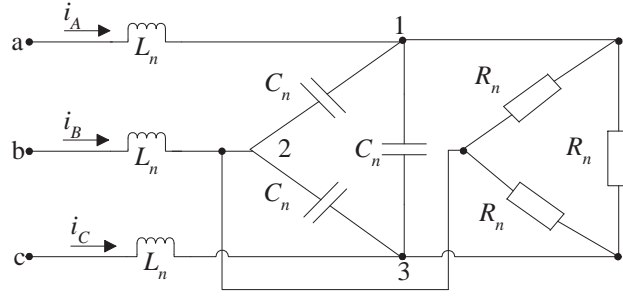


Figure 3.9: Ac-side of three-phase inverter connected to delta-connected load.

Figure 3.10 depicts three identical single-phase systems. Inductor current i_A has two components i_{c1} and i_{l1} .

$$i_{c1} = i_A \sin \theta \quad (3.6)$$

$$i_{l1} = i_A \cos \theta \quad (3.7)$$

For $L_n = 5$ mH, $C_n = 20$ μ F and rated current $i_A = 10$ A, R_n is found to be 54 Ω . Thus,

$$R_n \geq 54 \Omega \text{ for } i_A \leq 10 \text{ A} \quad (3.8)$$

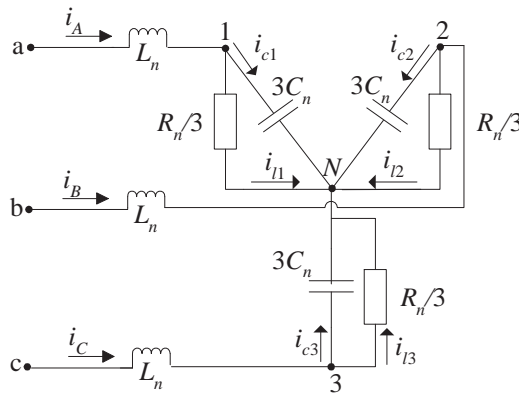


Figure 3.10: Simplified AC-side of three-phase inverter.

3.3.2 Control Stage

The control stage contains signal conditioning circuits, the PWM control circuit, MATLAB/Simulink, dSPACE (1103) hardware and software tools. The signal conditioning circuit boards convert power quantities (voltages and currents) to low level signals, which are compatible with dSPACE (1103) ADC channels. The dSPACE (1103) is specifically designed for development of high speed multi-variable digital controllers and real-time simulations in various fields. It is a complete real-time control system, based on a Power-PC processor. For advanced I/O purposes, it includes a slave-DSP (digital signal processing) subsystem based on TMS320F240 micro-controller.

dSPACE (1103)

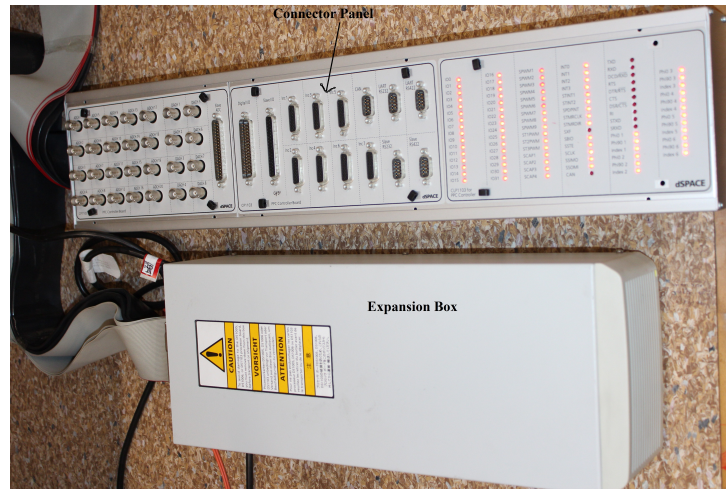


Figure 3.11: dSPACE (1103) hardware setup.

Figure 3.11 shows a dSPACE (1103) hardware setup. A description of the dSPACE real-time simulator is presented in Figure 3.12. The hardware is composed of a processor card DS1103, a connector panel CLP1103, an expansion box PX4 and linking boards between the host computer and processor card.

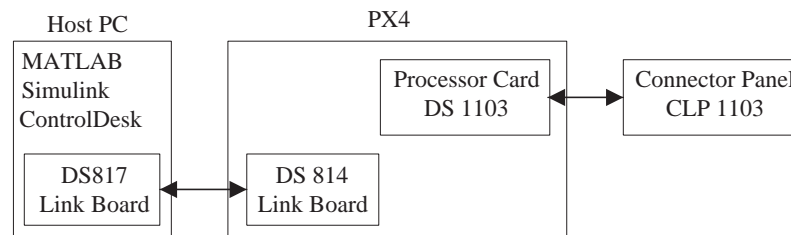


Figure 3.12: dSPACE interface details.

ControlDesk is the dSPACE experiment software. This software serves multiple purposes. It provides a platform for downloading controller models designed in Simulink onto the DSP. The “instrument panel” feature of ControlDesk is used to display various measurements such as the voltages and currents from the converter, reference signal, error signal and/or PWM signal *etc.* Some inputs, such as the converter voltages and currents could be sent through the CLP1103 and DS1103 before the measurements are displayed in ControlDesk on the host computer. The expansion box(PX4) houses the DS1103.

The CLP1103 connector panel provides an interface between the DS1103 and external real-time system hardware. The CLP1103 connector panel contains 28 BNC connectors, 20 for analogue

inputs and 8 for analog outputs, and several other connectors that can be used for digital I/O, slave/DSP I/O, incremental encoder interfacing, Controller Area Network (CAN) interfacing, and serial interfacing. Only Analogue to Digital Converter (ADC), Digital to Analogue Converter (DAC) and the Slave I/O (for PWM output) interfaces are used in experimental investigations. Technical details of dSPACE (1103) are given in Table 3.4 [76].

Table 3.4: Technical details of dSPACE (1103).

Parameters		Specifications
Processor	PowerPC Type	PPC 750GX
	CPU Clock	1 GHz
	Bus Frequency	133 MHz
Memory	Local memory	32 MB application SDRAM
	Global memory	96 MB communication SDRAM for data storage and exchange with host
Timer	2 General purpose timers	one 32-bit down and one 32-bit up counter
	1 Sampling rate timer	32-bit down counter
	1 time base counter	64-bit up counter
Interrupt controller		20 interrupts
A/D converter	Channels	16 multiplexed channels and 4 parallel channels
	Input Voltage range	± 10 V
	Overvoltage protection	± 15 V
	SNR	≥ 83 dB
	Offset error	± 5 mV
D/A converter	Channels	8 channels
	Output range	± 10 V
	Offset error	± 1 mV
	SNR	≥ 83 dB
Digital I/O	Channels	32-bit parallel I/O organized in four 8-bit groups
	Voltage range	TTL input/output levels
Incremental Encoder	Channels	6 digital channels and 1 analogue channel

The ControlDesk provides an interface for downloading controller models designed in Simulink onto the DSP.

Signal Conditioning Circuit Boards

The voltage and current conditioning circuit boards in Figure 3.1 have two stages; signal sensing and signal conditioning stage.

Signal Sensing Stage: Conversion of power quantities to low level signals is achieved by using Hall-Effect voltage and current transducers. The Hall-Effect voltage transducer LEM LV 25-P and current transducer LEM LA 55-P are used.

For both transducers the output voltage is obtained across an external resistance R_M . In this application, three voltage transducers (two for line-to-line ac voltages and one for dc bus voltage) and three current transducers (for inductor currents) have been used. The circuit and design details for voltage and current transducers are shown in Figure 3.13(a) and 3.13(b) respectively.

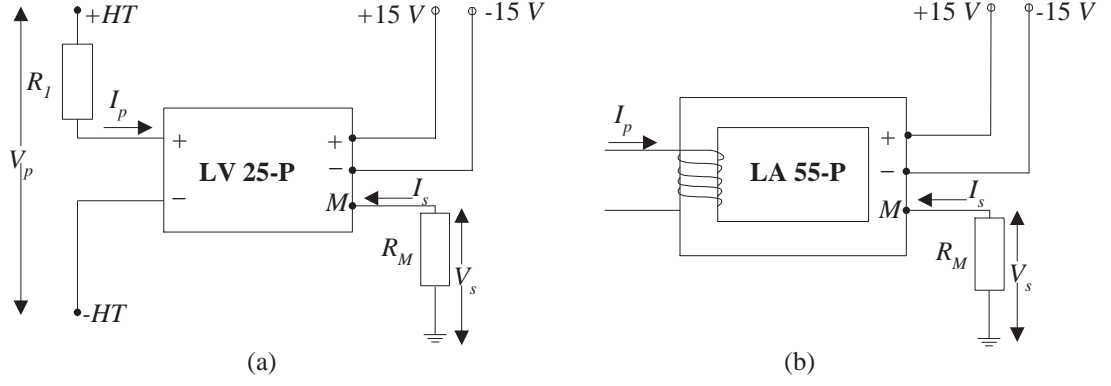


Figure 3.13: Signal sensing circuit (a) Voltage transducer LV 25-P (b) Current transducer LA 55-P.

Voltage Sensing Circuit: The optimum accuracy of LV 25-P is obtained at the nominal primary current $I_p = 10 \text{ mA}$ [77]. R_1 is calculated such that the nominal voltage to be measured V_p generated a current $I_p = 10 \text{ mA}$.

$$R_1 = \frac{V_p}{I_p} - R_p \quad (3.9)$$

where $R_p = 250 \text{ } \Omega$ is the resistance of primary coil. The $R_1 = 10.75 \text{ k}\Omega/3 \text{ W}$ for output ac voltage (110 V rms) measurement, whereas $R_1 = 39.75 \text{ k}\Omega/6 \text{ W}$ for dc bus voltage (400 V) measurement. The secondary current I_s is calculated as:

$$I_s = \frac{N_p}{N_s} I_p = 0.025 \text{ A} \quad (3.10)$$

where conversion ratio $= N_p/N_s = 2500 : 1000$. The output measuring resistance is taken as $R_M = 274 \text{ } \Omega$ therefore the secondary voltage V_s is

$$V_s = I_s R_M = 6.85 \text{ V rms} \quad (3.11)$$

Current Sensing Circuit: The circuit connection for the Hall Effect current transducer is shown in Figure 3.13(b) [78]. In the experimental setup, the current of $\pm 10 \text{ A}$ (peak) is converted to $\pm 6 \text{ V}$ (peak). Four turns are wound to carry a 40 AT mmf in the primary winding. With the conversion ratio of 4:1000, the secondary current I_s is given by:

$$I_s = \frac{N_P}{N_S} I_P = 0.04 \text{ A} \quad (3.12)$$

The secondary voltage V_s across $R_M = 150 \text{ } \Omega$ is:

$$V_s = I_s R_M = 6 \text{ V (peak)} \quad (3.13)$$

Signal Conditioning Stage: To better utilize the voltage range of dSPACE's ADCs and for better measurement accuracy, a signal conditioning stage is developed. The conditioning circuit is shown in Figure 3.14. This circuit contains three operational amplifiers, first one is acting as buffer, and the remaining two are inverting amplifiers. The second amplifier provides a suitable gain to the input signal, so that the output signal is in the safe and acceptable range of ADCs. LM324 has been used in signal conditioning stages of voltage and current measurement boards.

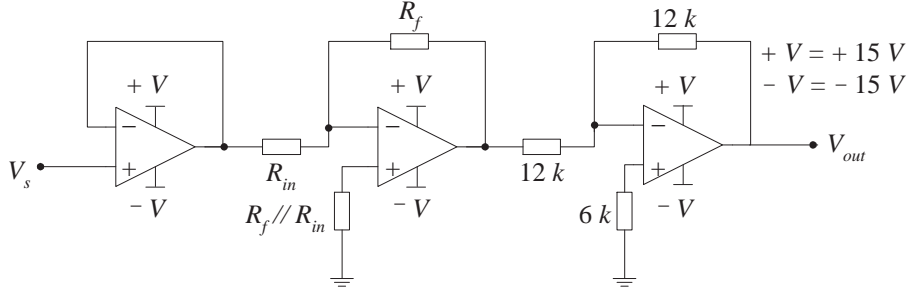


Figure 3.14: Signal conditioning circuit.

The resistances R_f and R_{in} determine the gain of the circuit according to the following equation

$$A_v = -\frac{R_f}{R_{in}} \quad (3.14)$$

$$V_{out} = A_v V_s \quad (3.15)$$

Table 3.5 lists different parameters values of signal conditioning stage for both voltage and current conditioning circuits.

Table 3.5: The details of signal conditioning circuit boards.

Board	V_s (V peak)	R_f (Ω)	R_{in} (Ω)	A_v	V_{out} (V peak)
Voltage conditioning board	9.69	11800	14000	0.84	8
Current conditioning board	6	11800	8870	1.33	8

PWM Control Board

The dSPACE (DS1103) can generate symmetric or asymmetric PWM signals. Symmetric PWM signals with fixed sampling rate have been generated and used in all experimental investigations performed in this research work. It means that all the signals have been sampled in the center of the PWM signal. In simulation the sampling of signals can be done a little random as well but in practical implementation using dSPACE only fixed sampling can be used. The dSPACE generated three logic level PWM signals (PWM_1 , PWM_2 , and PWM_3) and I/O enable control signal are passed to PWM control board. A simplified diagram of the PWM Control board is shown in Figure 3.15.

The PWM control board provided six logical outputs ($PWM TOP_1$, $PWM BOT_1$, $PWM TOP_2$, $PWM BOT_2$, $PWM TOP_3$, and $PWM BOT_3$) compatible with the SEMIKRON driver circuit. These PWM signals are blocked by the PWM control board in the event of an error. The PWM control board provided following three types of protection against faults:

- PWM signals are automatically blocked if any of the Error signals from inverter indicated error.
- PWM signals are automatically blocked if controller indicated any error using I/O enable.
- Manual On/Off control switch for protection under any unexpected/fault situation.

The output PWM signals from the PWM control board are then provided to the driver section of the SEMIKRON converter system. The IGBT driver section shown in Figure 3.4 controls and protects the IGBT switches and the user by:

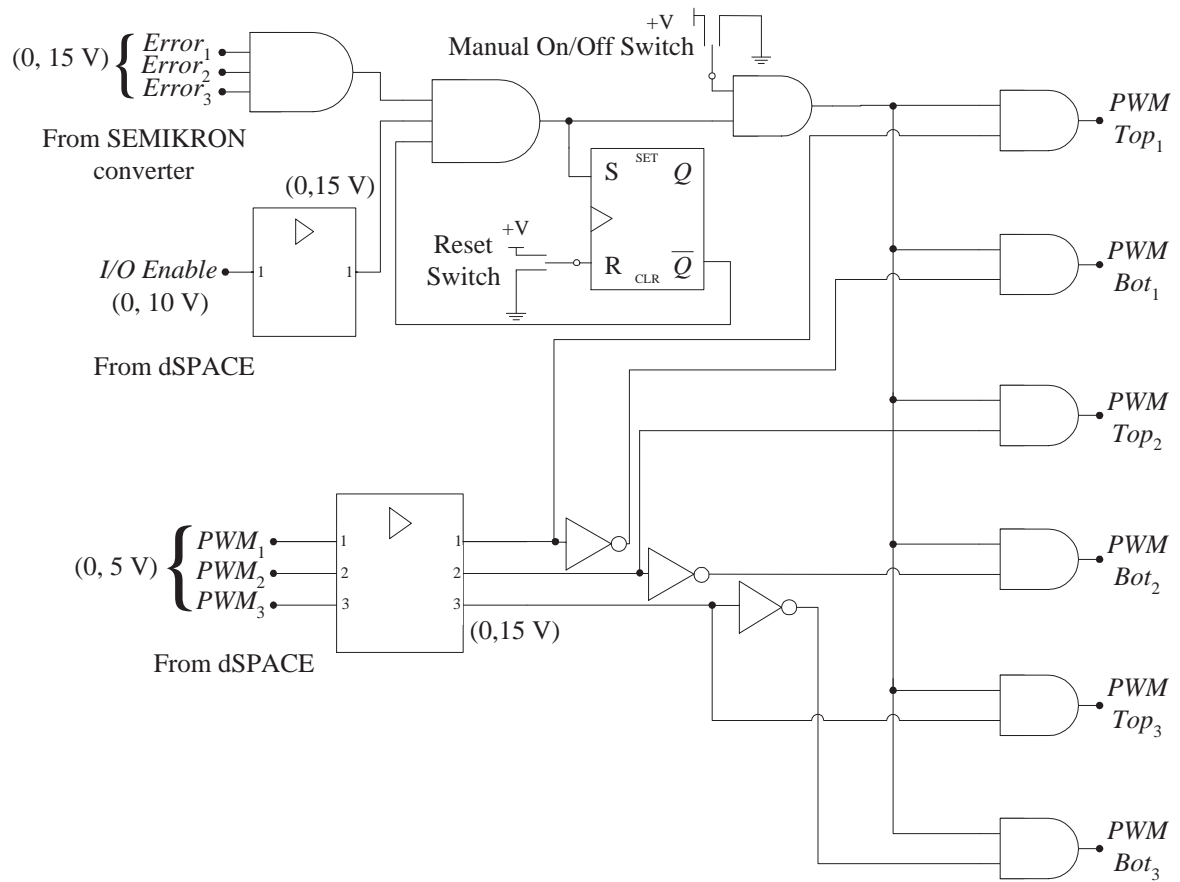


Figure 3.15: Simplified diagram of PWM control board.

- Amplifying the logic signals to deliver high peak current to the gate terminals of the IGBTs
- Monitoring the errors
- Interfacing and isolating the primary circuit (low power) from secondary circuit (high power)

The error signals from the converter are negative logic signals. In the event of error the related error signal switches from 15 V to ≈ 0 V. The PWM control board monitored the error signals and automatically blocks the PWM signal in case of an error. The signal remained blocked until a reset button is pressed. An SR latching circuit is used to block/clear the PWM signals.

For single-phase converter experiments, a single-phase PWM circuit board is developed separately. The design of single-phase PWM board is very similar to the design of three-phase PWM circuit board. A separate board is needed as the PWM signals in case of single-phase and three-phase PWM generation are available on different pins of slave Slave I/O connector and these pins are fixed on the board.

Complete circuit diagrams of all the boards are included in Appendix B.

3.4 CONCLUSION

In this Chapter the details of converter design, implementation and associated boards such as voltage/current conditioning circuit boards and PWM control boards are presented. The details of conversion of high power signals to/from low level signals which are acceptable by the control environment (dSPACE 1103) have also been presented. The design of the test rig presented in this Chapter is given from the point of view of three-phase converter implementations however it is also used for single-phase converter implementations.

Chapter 4

DESIGN AND ANALYSIS OF FRACTIONAL ORDER REPETITIVE CONTROLLERS

4.1 INTRODUCTION

It has already been shown in Chapter 2 that Conventional Repetitive Controllers (CRC) are not capable of working under varying frequency conditions. The literature dealing with the issue of varying frequency leading to a non-integer ratio (N_o) between the sampling frequency (f_s) and the fundamental frequency of the reference signal (f) can be divided into two categories: using a variable sampling time RC controller whose sampling time varies according to reference/disturbance signal period to maintain an integer ratio N_o , or using a frequency adaptive RC control schemes with fixed sampling time.

Frequency adaptive RC control schemes with fixed sampling time can be further divided into two groups: fixed sampling rate RC controller followed by a fictitious sampler operating at variable sampling rate, and Fractional Delay (FD) filter based RC controllers. This research work falls in the category of fractional delay filter based RC controllers. Fractional delay filter based RC control is a relatively new approach, with the first research paper published in 2007 and only a few papers published since then [54, 72, 79, 80]. Therefore, there is lot of opportunity to further establish this area.

Use of FD filter based RC controllers to deal with the issue of variable frequency signals in power converters has been referred as Fractional Order Repetitive Control (FORC) of power converters. FORC controllers used in the literature usually employ finite impulse response (FIR) FD filters to generate the required fractional delay. This chapter suggests a FORC controller design modification to enhance the stable operating range of the FORC controller. The design procedure explained in [72, 79] works well if the FD filter order is chosen to be unity. However, increasing the order of FD filter may result in a reduced stability range and sometimes unstable operation of the overall system.

This Chapter describes modification in the design of the FORC controller by optimizing the fractional delay filter. The key point of the improvement lies in the fact that the proposed design method uses an optimized FD filter that yields a unity magnitude response and a constant fractional delay throughout the bandwidth of the FD filter for any order ($n = 1, 2, 3 \dots$) of the filter. It also describes the tools developed with the aim of analyzing the stability of the FORC controlled system working under fixed sampling rate and variable frequency reference signal conditions.

In this chapter state-of-the-art research is explained in Section 4.2. Section 4.3 explains the issues that may arise with the existing FORC design procedures and it also describes enhancement/improvement in the design of FORC controller. Stability criteria of the FORC control system have also been developed in this section. In Section 4.4 a FORC controller has been developed using optimized FD filter based FORC design technique, for a single-phase PWM

dc/ac converter, and experimental results show the effectiveness of design approach. Finally the conclusion is given in Section 4.5

4.2 STATE-OF-THE-ART RESEARCH

Based on the Internal Model Principle (IMP), many controllers have been developed for grid connected converters *e.g.* repetitive controllers [55, 81–83], resonant controllers [46, 60, 84–87] and hybrid controllers [49, 84, 88]. The IMP based controllers offer accurate control of periodic signals as the internal model of the reference signal is included in the stable closed-loop. However, optimal mitigation of certain harmonics is still very difficult to achieve. For example, conventional RC schemes include the model of the reference signal at the fundamental and all harmonic frequencies below the Nyquist frequency. However, the control gain at fundamental and all harmonic frequencies is same and thus these control schemes fail to optimally suppress selective harmonic frequencies. Considering the harmonic distribution, multiple parallel structure resonant controller also referred as MRSC, and Discrete Fourier Transform based RC (DFT-RC) at selected harmonic frequencies with independent control gains offer fast transient response at the cost of heavy computational cost.

To avoid high computational burden of MRSC and DFT-RC, an IMP based Selective Harmonic Control (IMP-SHC), also called $(nk \pm m)$ -order harmonic RC, is used. It includes internal models of $(nk \pm m)$ ($m \leq n/2$ and n is the pulse number) order harmonics to optimally mitigate selected harmonics [47, 51]. A dual-mode RC control scheme which is a special case of DFT-RC has also been used in the control of grid connected converters. However, all these techniques are sensitive to frequency variations *i.e.* the harmonic frequencies of the controller and reference signal do not match, leading to higher tracking error, increased THD and poor performance.

To deal with this issue of frequency variations two possibilities have been considered in the literature: one is to use variable sampling rate and the other is by employing FD filters. The variable sampling time techniques are seldom used due to their implementation complexity, time varying structure of the controller and other issues like stability [53, 54]. Recently, FD filter based RC control schemes have been used in the control of converters, shunt active power filters and front ends [72, 79]. A Frequency Adaptive Hybrid Selective Harmonic Control (FA-SHC) scheme is also proposed by Yang *et.al.* This technique (FA-SHC) is based on the integer-period $(nk \pm m)$ -order harmonic RC [80]. Compared with the conventional RC and the $(nk \pm m)$ -order harmonic RC, the control gains of the FA-SHC can be optimally weighted to achieve desirable harmonic mitigation in grid connected inverter systems.

4.3 FRACTIONAL DELAY FILTER BASED REPETITIVE CONTROL SCHEMES

4.3.1 Optimal FD Filter Design

According to the Lagrange interpolation based FD filter design method, any fractional delay z^{-N_o} can be well approximated by FD filters with integer delays [89–93]. Like CRC, the order $N_o = f_s/f$ denotes the control resolution of FORC. Higher sampling frequencies normally lead to higher control accuracy.

The FORC technique reported previously [54, 72, 79, 80] assumes that $z^{-N_o} = z^{-(N_i+F)}$ with $N_i = \text{int}[N_o]$ being the integer part of N_o and $F = N_o - N_i$, $0 \leq F < 1$ being the fractional part of N_o . The fractional delay z^{-F} can be approximated by a Lagrange interpolation polynomial as follows [54, 79, 92]:

$$z^{-F} \approx \sum_{k=0}^n A_k z^{-k} \quad (4.1)$$

where n is the degree of the polynomial and the Lagrange coefficients A_k can be calculated as:

$$A_k = \prod_{\substack{i=0 \\ i \neq k}}^n \frac{F-i}{k-i} \quad k = 0, 1, 2, \dots, n \quad (4.2)$$

The case $n = 1$ corresponds to linear interpolation between two samples. The ideal magnitude response of z^{-F} is unity for all frequencies, and the phase response is linear with a slope of $-F$. Figure 4.1 shows the magnitude response and phase delay of first, second and third order Lagrange interpolation based filters for various fractional delay values $F = 0 \sim 0.9$. It is seen that bandwidth of (4.1) is 50%, 63% and 75% of the Nyquist frequency for $n = 1$, $n = 2$ and $n = 3$ respectively, *i.e.* higher order fractional delay filter brings larger bandwidth and better approximation of fractional delay z^{-F} in the low frequency band.

A FD filter must be able to meet two main frequency-domain specifications. The filter's magnitude response must possess an all-pass behavior in a wide frequency range, and its phase response must be linear with a slope $-F$ throughout the bandwidth of the filter. A linear phase response with a slope $-F$ within the bandwidth of the filter ensures that the phase delay is F samples throughout the bandwidth. From Figure 4.1 it can be seen that phase delay response of second and third order FD filter is not really constant within their bandwidth. The magnitude response of a third order FD filter also overestimates the amplitude of the signal which may lead to the overall instability or at least the reduced stability range of the system. Section 4.3.3 explains how the overestimation of the amplitude of the signal can lead to instability of the system. However, if the signal is not overestimated but the phase delay is not constant within the bandwidth then the phase difference between the actual and estimated signal gives rise to error. Increasing error in a certain period might increase the transient time of the controller and thus zero steady-state error would be achieved in longer time. Therefore in case of $0 \leq F < 1$ only first order FD should be utilized which has close to unity signal amplitude and constant phase delay within the bandwidth.

The approximation remainder term of the Lagrange interpolation can be derived as follows:

$$R_n = z^{-F} - \sum_{k=0}^n A_k z^{-k} = \frac{\xi^{-F-n} \prod_{i=0}^{n-1} (-F-i)}{(n+1)!} \prod_{i=0}^n (F-i) \quad (4.3)$$

where $\xi \in [T_{sk}, T_{s(k+1)}]$ with T_{sk} and $T_{s(k+1)}$ being the k^{th} and $k+1^{th}$ sampling instants, respectively. Equation (4.3) shows that the approximation error decreases as the order of the interpolation increases. By increasing the polynomial degree n of the interpolator, a more accurate approximation can be acquired. However, higher order (2^{nd} and 3^{rd} order) filters shown in Figure 4.1 need to be optimized to have unity magnitude and constant phase delay within the bandwidth of the filter. Dutta suggested that approximation error for FD filter is smallest if the required fractional is in the optimal range [94]. The optimal delay range for an FD filter is given by [94]:

$$\frac{n-1}{2} \leq F \leq \frac{n+1}{2} \quad (4.4)$$

According to (4.4), for a third order ($n = 3$) FD filter, delay parameter F should be lying between 1 and 2 *i.e.* $1 \leq F \leq 2$. Figure 4.2 plots the magnitude and phase delay response of a third order FD filter when the fractional delay lies within its optimal delay range. It shows that choosing the fractional delay within the optimal delay range of the FD filter ensures that the amplitude of the signal is never overestimated and the phase delay is F samples within the bandwidth of the filter. It is also seen that magnitude response for fractional delay F and $n - F$ are the same. It can be concluded that for higher order FD filters, optimum fractional delay can be more than one sampling period. RC controllers used for power converter applications need

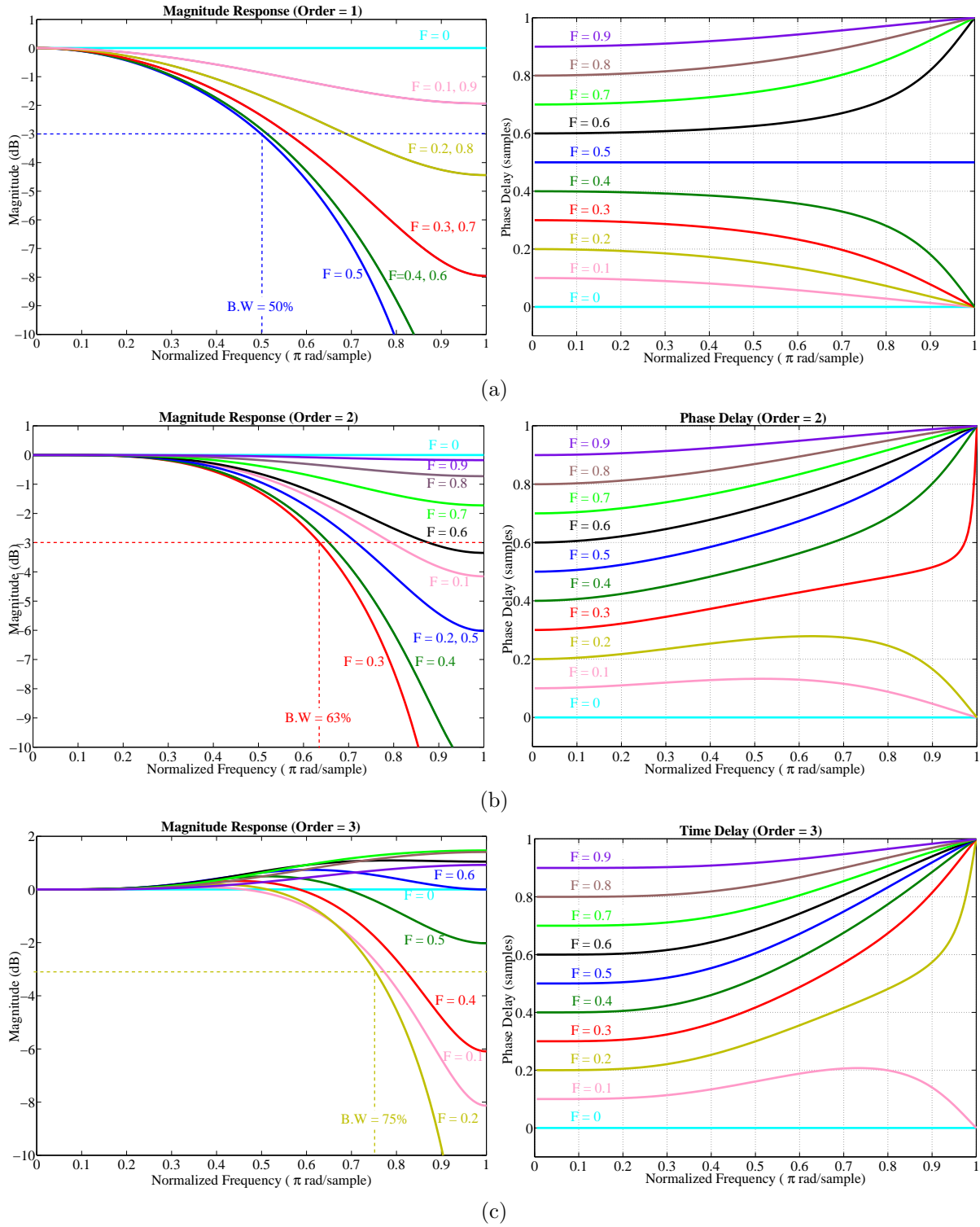


Figure 4.1: Frequency response of Lagrange interpolation based FD filters for a fractional delay range ($F = 0 : 0.1 : 0.9$): (a) $n = 1$ (b) $n = 2$ (c) $n = 3$.

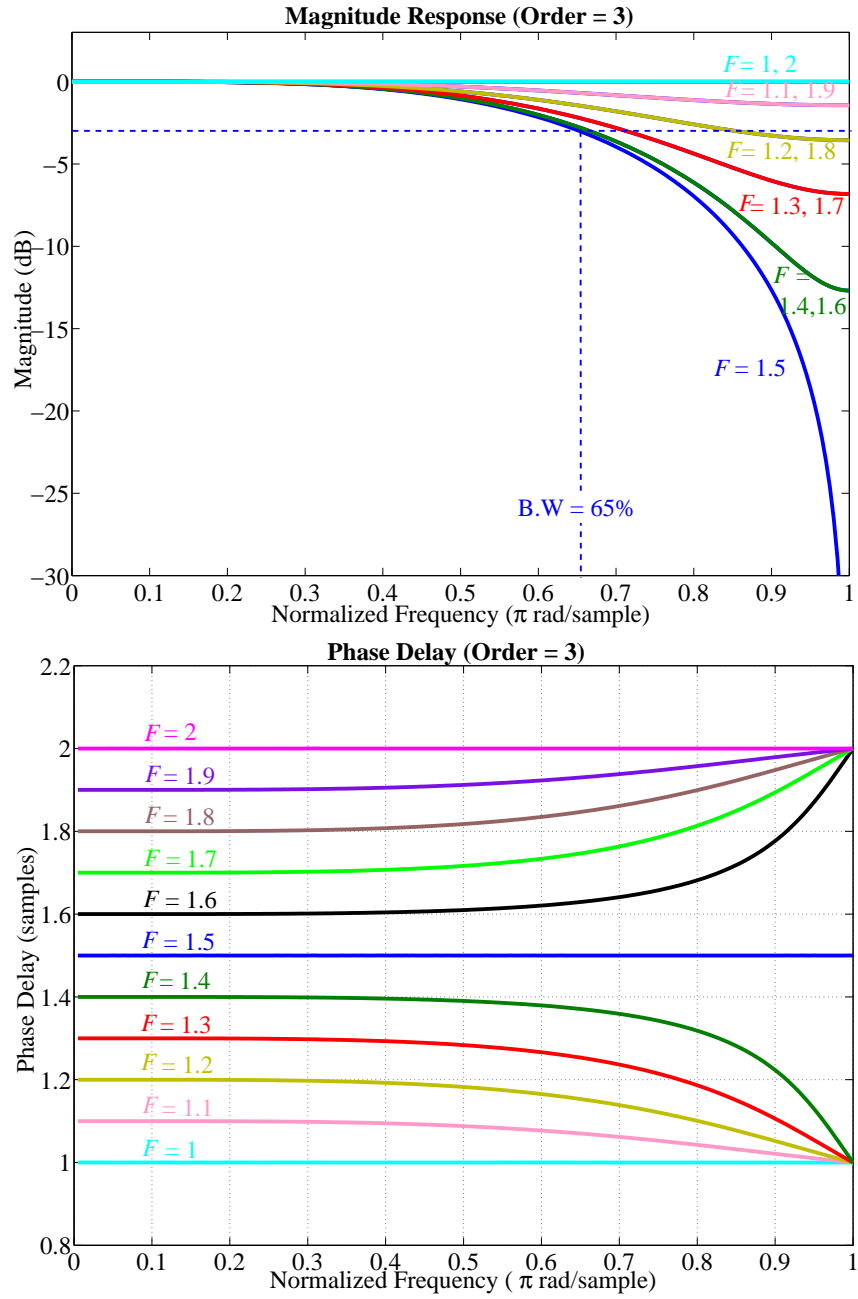


Figure 4.2: Frequency response of Lagrange interpolation based third-order FD filter for optimal fractional delay values ($1 \leq F \leq 2$).

an overall sample delay equal to the number of samples in one period of a reference signal which is usually quite high. This required sample delay can be divided in two parts N_i (still high) and F which is usually quite small.

It can be concluded that either only first order FD filter should be used with $0 \leq F < 1$ or that the required fractional delay F should be adjusted to be in the optimal delay range for least approximation error and better stability. The effect of a non-optimal FD filter upon the stability of the overall system is discussed in Section 4.3.3. The stability analysis presented in Section 4.3.3 also becomes a lot more easier if the FD filter magnitude response is unity within its bandwidth.

The optimal FD filter design procedure can be described as follow:

- Calculate $N_o = f_s/f$, where N_o is the order of the overall FORC controller.
- Select the order n of the FD filter. Usually first, second or third order filters are sufficient for most application in the area of converter control and signal processing.¹
- Calculate the required fractional delay F .

$$F = N_o - \left(\text{int}[N_o] - \frac{n}{2} \right) \quad \text{If } n \text{ is even} \quad (4.5)$$

$$F = N_o - \left(\lfloor N_o \rfloor - \left\lfloor \frac{n}{2} \right\rfloor \right) \quad \text{If } n \text{ is odd} \quad (4.6)$$

where $\lfloor \cdot \rfloor$ represents the floor function.

- Calculate the required integer delay $N_i = N_o - F$.
- Calculate FD filter co-efficients using (4.2).
- FD filter can be implemented using equation (4.1).

The Lagrange interpolation based FD filter structure is shown in Figure 4.3 and can be written as:

$$G_f(z) = A_0 + A_1 z^{-1} + A_2 z^{-2} + \dots + A_n z^{-n} = \sum_{k=0}^n A_k z^{-k} \quad (4.7)$$

4.3.2 Design of Fractional Order Repetitive Controller

A plug-in repetitive controller structure has been explained in Section 2.3.2. A conventional plug-in RC always demands an integer order *i.e.* N_o needs to be integer under all circumstances. However, in practice the grid frequency which is acting as a reference signal to be tracked in case of grid connected converters is varying uncontrollably.

Section 2.3 explains that the realization or internal model of a periodic reference signal of period $T = 1/f$ at a fixed sampling frequency f_s can be achieved by $N_o = f_s/f$ integer delays. Here a non-integer N_o is divided into two parts N_i and F *i.e.* $z^{-N_o} = z^{-(N_i+F)}$. The plug-in RC structure containing the internal model of a periodic reference signal is shown in Figure 2.12. A

¹To select the order n of the FD filter, a trade-off is made between the complexity and accurate approximation of the filter. That is to say lower order FD filter results in lower complexity and approximation of the required fractional delay is not very accurate. According to (4.3) approximation error can be reduced by increasing the order of the filter which also results in high computational complexity. Therefore, the FD filter order selection can be made depending upon the type of application. Like in communication and signal processing applications, usually higher order filters are used as a very accurate approximation of the delay is required.

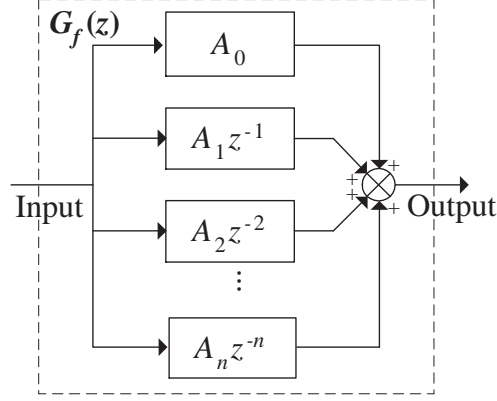


Figure 4.3: Lagrange interpolation based FD filter structure.

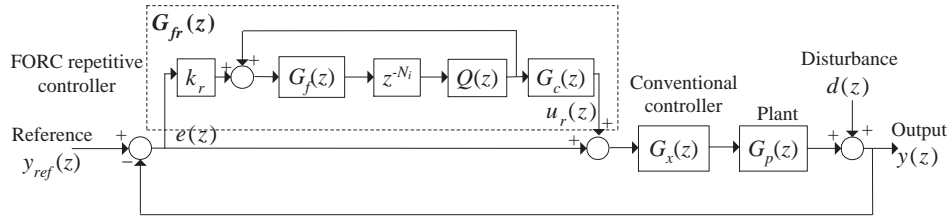


Figure 4.4: FORC control system.

FORC control system can be achieved by including an FD filter $G_f(z)$ along with z^{-N_i} inside the loop of the RC in Figure 2.12. A block diagram of a FORC controller is shown in 4.4.

The transfer function of FORC controller $G_{fr}(z)$ (Figure 4.4) is give by:

$$G_{fr}(z) = k_r \frac{G_f(z)(z^{-N_i}Q(z))}{1 - G_f(z)(z^{-N_i}Q(z))} G_c(z) \quad (4.8)$$

Substituting (4.7) in (4.8)

$$G_{fr}(z) = k_r \frac{z^{-N_i} \left(\sum_{k=0}^n A_k z^{-k} Q(z) \right)}{1 - z^{-N_i} \left(\sum_{k=0}^n A_k z^{-k} Q(z) \right)} G_c(z) \quad (4.9)$$

where A_k s are defined by F as shown in (4.2). The fractional order repetitive control of (4.9) for $F = 0$ becomes equivalent to the CRC. Thus the FORC provides a general approach for tracking or elimination of any periodic signal, with an arbitrary fundamental frequency, resulting in integer or non-integer value of N_o .

The output signal $y(z)$ in Figure 4.4 is given by:

$$y(z) = \frac{y_{ref}(z)(1 + G_{fr}(z))G_x(z)G_p(z) + d(z)}{1 + (1 + G_{fr}(z))G_x(z)G_p(z)} \quad (4.10)$$

From Figure 4.4 the transfer functions from $y_{ref}(z)$ and $d(z)$ to $y(z)$ in the overall closed-loop

system, are:

$$\begin{aligned} \frac{y(z)}{y_{ref}(z)} &= \frac{(1 + G_{fr}(z))G_x(z)G_p(z)}{1 + (1 + G_{fr}(z))G_x(z)G_p(z)} \\ &= \frac{\left\{1 - z^{-N_i} \left(\sum_{k=0}^n A_k z^{-k} \right) Q(z) (1 - k_r G_c(z)) \right\} H(z)}{1 - z^{-N_i} \left\{ Q(z) \left(\sum_{k=0}^n A_k z^{-k} \right) (1 - k_r G_c(z) H(z)) \right\}} \end{aligned} \quad (4.11)$$

$$\frac{y(z)}{d(z)} = \frac{(1 + G_x(z)G_p(z))^{-1} \left(1 - z^{-N_i} \left(\sum_{k=0}^n A_k z^{-k} \right) Q(z) \right)}{1 - z^{-N_i} \left(\sum_{k=0}^n A_k z^{-k} \right) Q(z) (1 - k_r G_c(z) H(z))} \quad (4.12)$$

where

$$H(z) = \frac{G_x(z)G_p(z)}{1 + G_x(z)G_p(z)} = \frac{z^{-d} B^+(z^{-1}) B^-(z^{-1})}{A(z^{-1})} \quad (4.13)$$

where $d \in \mathbb{R}$ is the known delay steps of the system, $B^+(z^{-1})$ and $B^-(z^{-1})$ are the cancelable and un-cancelable parts of the numerator, and $A(z^{-1}) = 0$ is the system characteristic equation. In order to achieve zero-phase compensation, the compensating filter $G_c(z)$ can be chosen as [40, 83, 95]:

$$G_c(z) = \frac{z^d A(z^{-1}) B^-(z^{-1})}{B^+(z^{-1}) b} \quad (4.14)$$

where $b \geq \| B^{-1}(z^{-1}) \|^2$. The delay steps d can be determined by experiments in practical applications.

4.3.3 Stability Criteria for FORC

There are various methods to examine the stability of a system but FORC due to its high degree of polynomial equation pushes each approach to its limit. For example, calculating the poles positions is the most common method for stability studies but FORC has a very high value of N_o (200 when $f = 50$ Hz and $f_s = 10$ k Hz) which makes root finding very complex for any root finding algorithm. Using the standard Nyquist stability criterion from (4.10) – (4.14), it can be concluded that the overall closed-loop system is stable if the following two conditions hold:

1) The closed-loop system without the FORC controller *i.e.* $H(z)$ (given in (4.13)) is asymptotically stable. That is to say, roots of $1 + G_x(z)G_p(z) = 0$ are inside the unit circle [45, 55].

2) $1 - z^{-N_i} \sum_{k=0}^n A_k z^{-k} Q(z) (1 - k_r G_c(z) H(z)) = 0$ has roots inside the unit circle, then

$$|Q(z)| \left| \sum_{k=0}^n A_k z^{-k} \right| |1 - k_r G_c(z) H(z)| < 1, \forall z = e^{j\omega} \quad (4.15)$$

Note that, both N_i and F change slowly with the grid frequency variations in practical applications, the magnitude response of z^{-N_i} is always unity, for all frequencies, as N_i is restricted to be an integer value only. Appropriate division of N_o into its two parts (N_i and F) ensures that the magnitude response of FD filter is always unity within the bandwidth of the filter if the value of F lies within the optimal fractional delay range of the FD filter. The optimal fractional delay range of any FD filter is given by (4.4). If the bandwidth of the proposed FD filter of (4.1) is larger than the bandwidth of the low pass filter $Q(z)$ in practical applications, then

$$\left| \sum_{k=0}^n A_k z^{-k} \right| \rightarrow 1 \text{ and } |Q(z)| \rightarrow 1$$

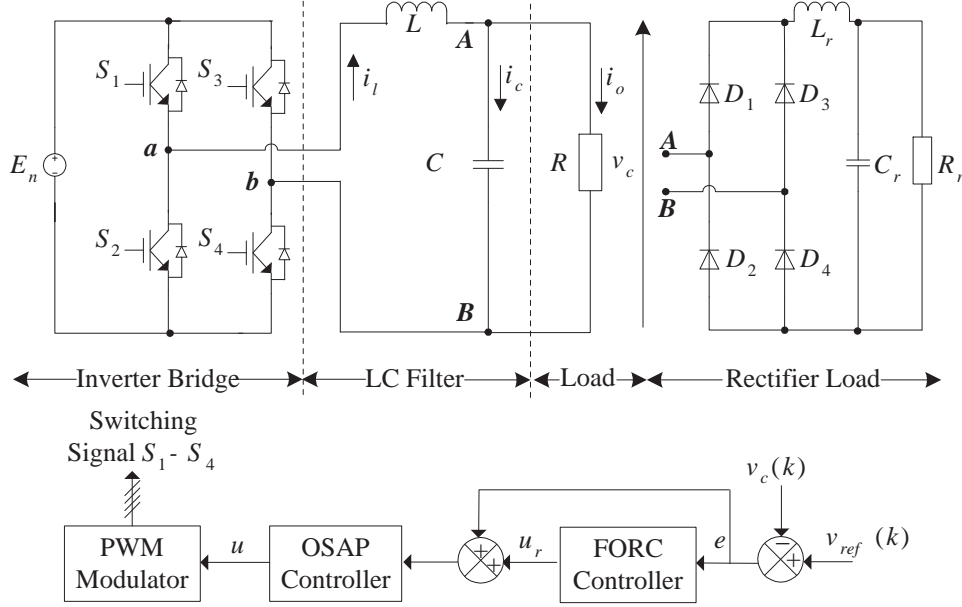


Figure 4.5: Block diagram of a FORC controlled single-phase inverter.

within the pass band of $Q(z)$. The stability criteria for CRC system has already been obtained in [67, 80]. The first stability condition of FORC is exactly the same as that for CRC systems; within the pass band of $Q(z)$ the stability criterion of (4.15) for FORC systems becomes equivalent to that for CRC systems. When $G_c(z)$ of (4.14) is applied to achieve zero-phase compensation, the stability range for the FORC gain is $0 < k_r < 2$. It is clear that the synthesis of FORC systems can be almost same as that of well-known CRC systems.

4.4 EXPERIMENTAL VALIDATION

4.4.1 Case Study: Single-Phase PWM Inverter

Figure 4.5 shows a single-phase, stand-alone voltage source FORC controlled PWM inverter. In this case it has been used to track a grid voltage reference signal which is a variable frequency signal. In this experiment, our aim is to measure the performance of a FORC controlled, stand-alone single-phase PWM inverter while tracking a variable frequency grid voltage signal. If the performance of the inverter is good it can be synchronized and connected to the grid.

The dynamics of the single-phase PWM inverter connected to a resistive load as shown in Figure 4.5, have been obtained in Appendix A, and is given by (A.21). The sampled-data equation of a single-phase inverter (A.21) is given by (A.25) [41, 45, 54]:

Considering the dc/ac converter described by (A.25) and its output equation $y(k) = v_c(k)$, the control objective is to force the output voltage v_c to track the sinusoidal reference signal v_{ref} (also referred as y_{ref}) in the presence of various uncertainties (load, parameter *etc.*) and frequency variations.

4.4.2 Design of Digital Controller

The controller for a single-phase PWM inverter is comprised of two parts: conventional feedback controller (OSAP) and FORC controller. The Auto Regressive Moving Average (ARMA)

Table 4.1: System parameters.

Nominal Values	Actual Values	Rectifier Load	Others
$E_n = 100 \text{ V}$	$E = 98 \text{ V}$	$R_r = 20 \Omega$	$v_{ref} = 50 \sin(2\pi ft) \text{ V}$
$R_n = 20 \Omega$	$R = 18 \Omega$	$L_r = 3 \text{ mH}$	$\alpha_0 = 0.5$
$C_n = 30 \mu F$	$C = 28 \mu F$	$C_r = 1100 \mu F$	$\alpha_1 = 0.25$
$L_n = 5 \text{ mH}$	$L = 3 \text{ mH}$		$f_s = f_{sw} = 10 \text{ kHz}$

Table 4.2: Control schemes.

Abbreviation	Control technique name
CRC _N	Conventional repetitive control with nominal order
CRC _T	Conventional repetitive control with order truncated to the nearest integer
FORC (n)	Fractional order repetitive control using non-optimal FD filter of order n
FORC _O (n)	Fractional order repetitive control using optimal FD filter of order n

equation for the dynamics of (A.21) can be derived as [41, 96]:

$$y(k+1) = -p_1 y(k) - p_2 y(k-1) + m_1 u(k) + m_2 u(k-1) \quad (4.16)$$

where $u(k) = \pm \Delta T(k)$, $p_1 = -\varphi_{11} - \varphi_{22}$, $p_2 = \varphi_{11}\varphi_{22} - \varphi_{12}\varphi_{21}$, $m_1 = g_1$ and $m_2 = \varphi_{12}g_2 - \varphi_{22}g_1$. Based on the system parameter values used in this experiment, $p_1 = -1.7806$, $p_2 = 0.8428$, $m_1 = 0.0333$, $m_2 = 0.0289$, and the plant parameters are: $\varphi_{11} = 0.9667$, $\varphi_{12} = 9.1667e^{-5}$, $\varphi_{21} = -611.11$, $\varphi_{22} = 0.8139$, $g_1 = 0.0333$ and $g_2 = 611.11$.

If the control law for the plant equation (4.16) is chosen as:

$$u(k) = \frac{1}{m_1} (y_{ref}(k) - m_2 u(k-1) + p_1 y(k) + p_2 y(k-1)) \quad (4.17)$$

then $y(k+1) = y_{ref}(k)$. It yields the deadbeat response with a transfer function $H(z) = z^{-1}$. Equation (4.17) describes a *One Sampling Ahead Preview* (OSAP) controller [96, 97]

In order to exactly track periodic reference signals of variable frequency, a plug-in FORC controller $G_{fr}(z)$ of (4.8) is plugged into the conventional feedback controlled inverter.

4.4.3 Experimental Results

Experimental investigations are carried out on a stand-alone dc/ac single-phase converter system, under different load conditions. The rapid prototyping control kit dSPACE ds1103 and Matlab/Simulink are employed. The details of the experimental setup and hardware design are given in Chapter 3. The parameters of the converter system are given in Table 4.1. The nominal value of frequency f is 50Hz, and $Q(z) = 0.25z^1 + 0.5 + 0.25z^{-1}$.

A series of experiments has been carried out to compare the performance of various control schemes in the presence of variable frequency reference signal. All the experiments are performed under non-linear load conditions, except where the load type is clearly and separately mentioned (Figure 4.8 and 4.9). Table 4.2 list the abbreviations and details of the control schemes used in these experimental investigations. The THD of the output voltage with the reference signal

Table 4.3: THD for various CRC and FORC controllers.

$f(Hz)$	$N_o = f_s/f$	THD of output voltage (%)				
		CRC _N	CRC _T	FORC ($n = 1$)	FORC ($n = 3$)	FORC _O ($n = 3$)
49	204.08	13.18	1.59	1.66	1.20	1.20
49.1	203.67	13.88	4.03	1.59	1.44	1.01
49.2	203.25	13.55	2.53	1.60	1.20	1.1
49.3	202.84	12.51	2.78	1.51	1.33	1.01
49.4	202.45	11.59	4.19	1.6	1.58	1.14
49.5	202.02	10.97	1.34	1.54	1.29	1.17
49.6	201.61	9.57	4.98	1.61	1.27	1.19
49.7	201.21	7.98	2.41	1.44	1.31	1.2
49.8	200.8	6.09	2.52	1.66	1.57	1.22
49.9	200.4	3.40	3.72	1.62	1.54	1.19
50	200	1.45	1.58	1.41	1.35	1.21
50.1	199.6	5.18	4.42	1.48	1.41	1.17
50.2	199.2	7.33	2.56	1.55	1.36	1.21
50.3	198.81	8.22	2.22	1.47	1.40	1.2
50.4	198.41	9.66	3.36	1.46	1.36	1.09
50.5	198.01	10.1	1.34	1.48	1.46	1.22
50.6	197.63	10.15	4.65	1.6	1.40	1.22
50.7	197.24	11.69	3.18	1.58	1.22	1.2
50.8	196.85	12.82	2.32	1.49	1.30	1.13
50.9	196.46	13.16	4.3	1.63	1.24	1.16
51	196.07	13.70	1.88	1.76	1.46	1.19

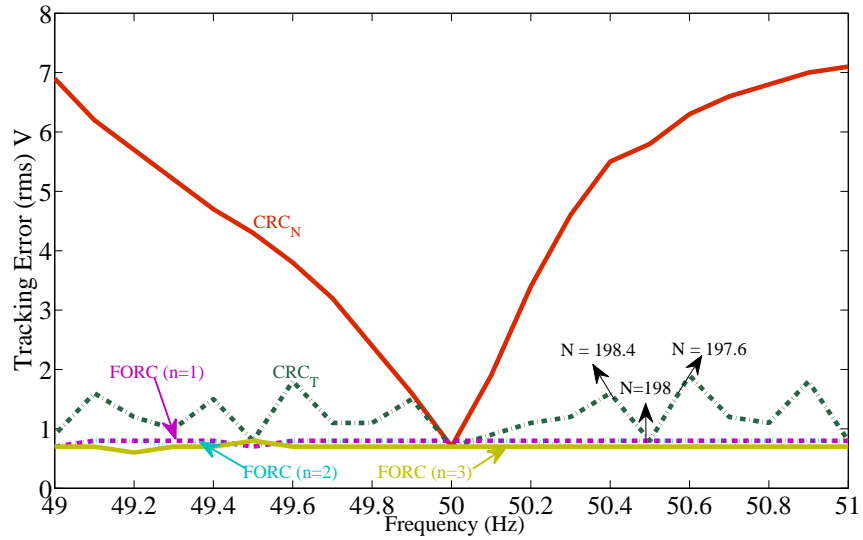


Figure 4.6: Steady-state tracking error for various control techniques.

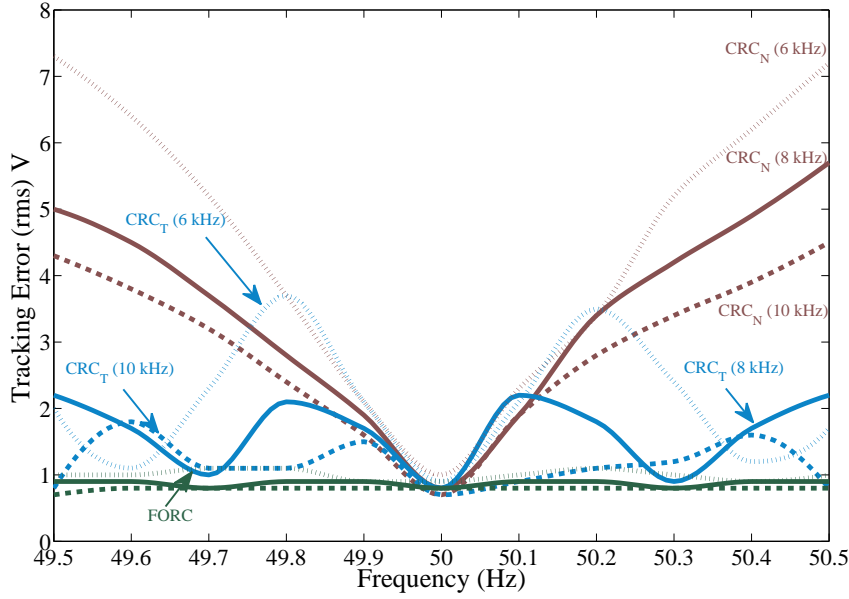


Figure 4.7: Sampling frequency effect on CRC and FORC control performance.

in the frequency range of 49Hz \sim 51Hz is tabulated in Table 4.3. THD given in Table 4.3 is the average THD of three cycles in steady-state. Experiments are run for one minute and THD present in the last three cycles is recorded. Table 4.3 indicates that the FORC control schemes yields the best tracking accuracy in terms of THD. Higher order FD filter in FORC control scheme reduces the THD value by a very small amount but the computational burden is also increased. Therefore there is a trade off between the computational burden and the THD value of output voltage. If a higher order FD is to be used it is better to use optimal FD filter based FORC represented by FORC_O in the last column of Table 4.3 as it yields the least THD value.

Figure 4.6 summarizes the steady-state tracking errors of the CRC and FORC controlled inverter, connected to non-linear load, in the frequency range of 49Hz \sim 51Hz. It is observed that the CRC_N is sensitive to frequency changes, the tracking error and the THD increases with frequency deviation $\Delta f = f - 50$ and the lowest tracking error value 0.7 V occurs at nominal frequency 50 Hz. CRC_T is actually a partial frequency adaptive RC scheme, which yields much better control accuracy than CRC_N does. The tracking error and the THD for CRC_N increases with $N_o - N_i \rightarrow 0.5$ and the lowest tracking error value 0.7 V occurs when $N_o = N_i$. Experimental results also show that FORCs with $n = 1, 2, 3$ are immune to frequency changes, their tracking errors almost keep a constant value around 0.7 V. Note that the theoretical analysis in 4.3.1 indicates that FORC with higher order FD filter will produce better tracking accuracy due to a larger bandwidth. However, in this case, the tracking error is mainly dominated by the low frequency harmonics so there is a very small difference in error generated by FORCs of different order FD filters.

Table 4.3 and Figure 4.6 clearly shows that FORC controlled inverter can precisely track the varying frequency sinusoidal signals at fixed sampling rate and yield very low steady-state error. Higher order FD filter based FORC can be employed to improve the tracking accuracy by removing high order harmonics if needed.

Figure 4.7 clearly demonstrates that the CRC_N control scheme is unable to track/reject periodic signals of variable frequencies at fixed sampling rate. However, the CRC_T control performance strongly depends upon sampling frequency. Higher sampling frequency leads to better control accuracy. It can be noted that the maximum rms tracking error at $f_s = 6$ kHz is very high (≈ 4 V), whereas the tracking error at $f_s = 10$ kHz is ≈ 2 V. Therefore, it can be concluded that

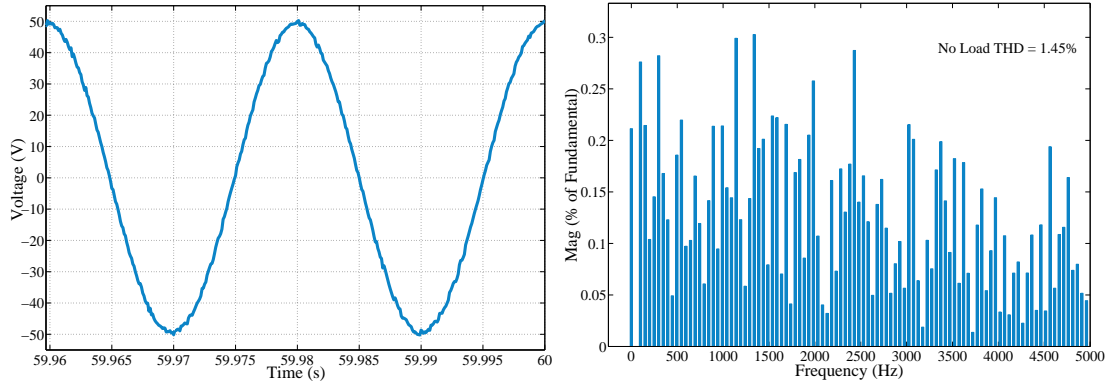
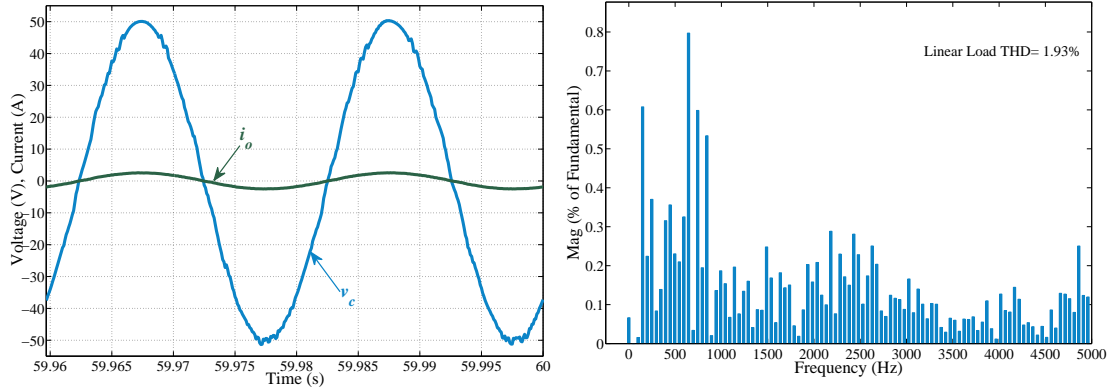
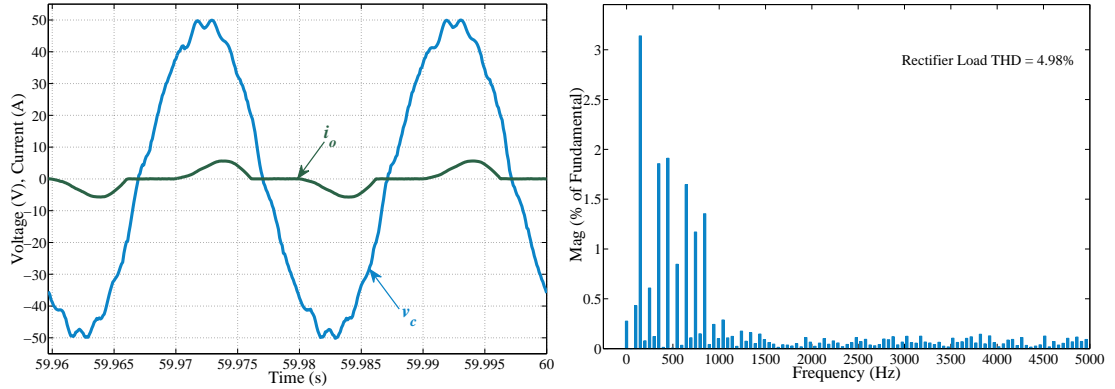
(a) v_c and its harmonic spectrum under no-load(b) v_c , i_o and harmonic spectrum of v_c under resistive load(c) v_c , i_o and harmonic spectrum of v_c under rectifier load

Figure 4.8: CRC_T controlled steady-state response under various loads when $f = 49.6\text{Hz}$ and $f_s = 10\text{kHz}$.

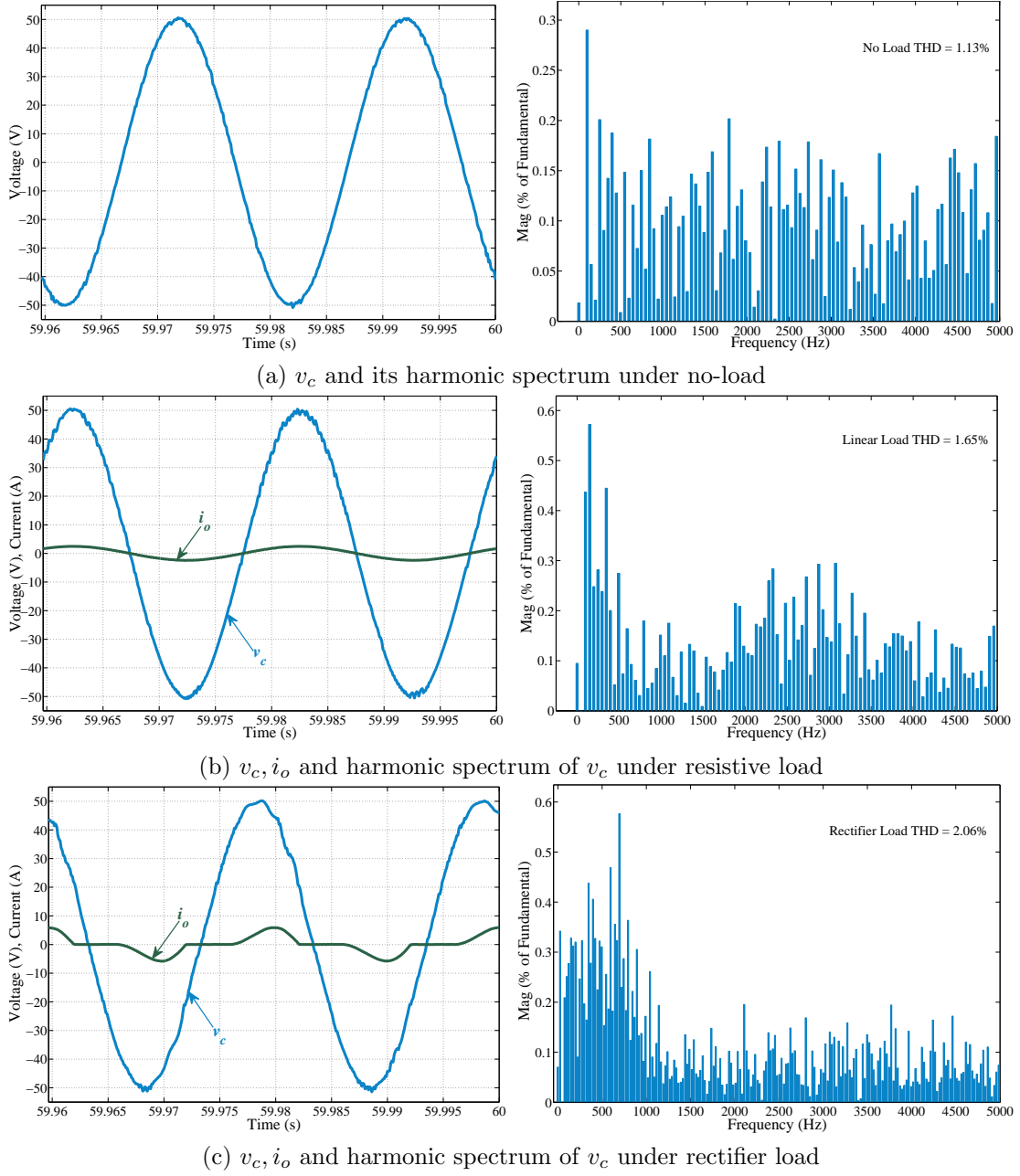


Figure 4.9: FORC controlled steady-state response under various loads when $f = 49.6\text{Hz}$ and $f_s = 10\text{kHz}$.

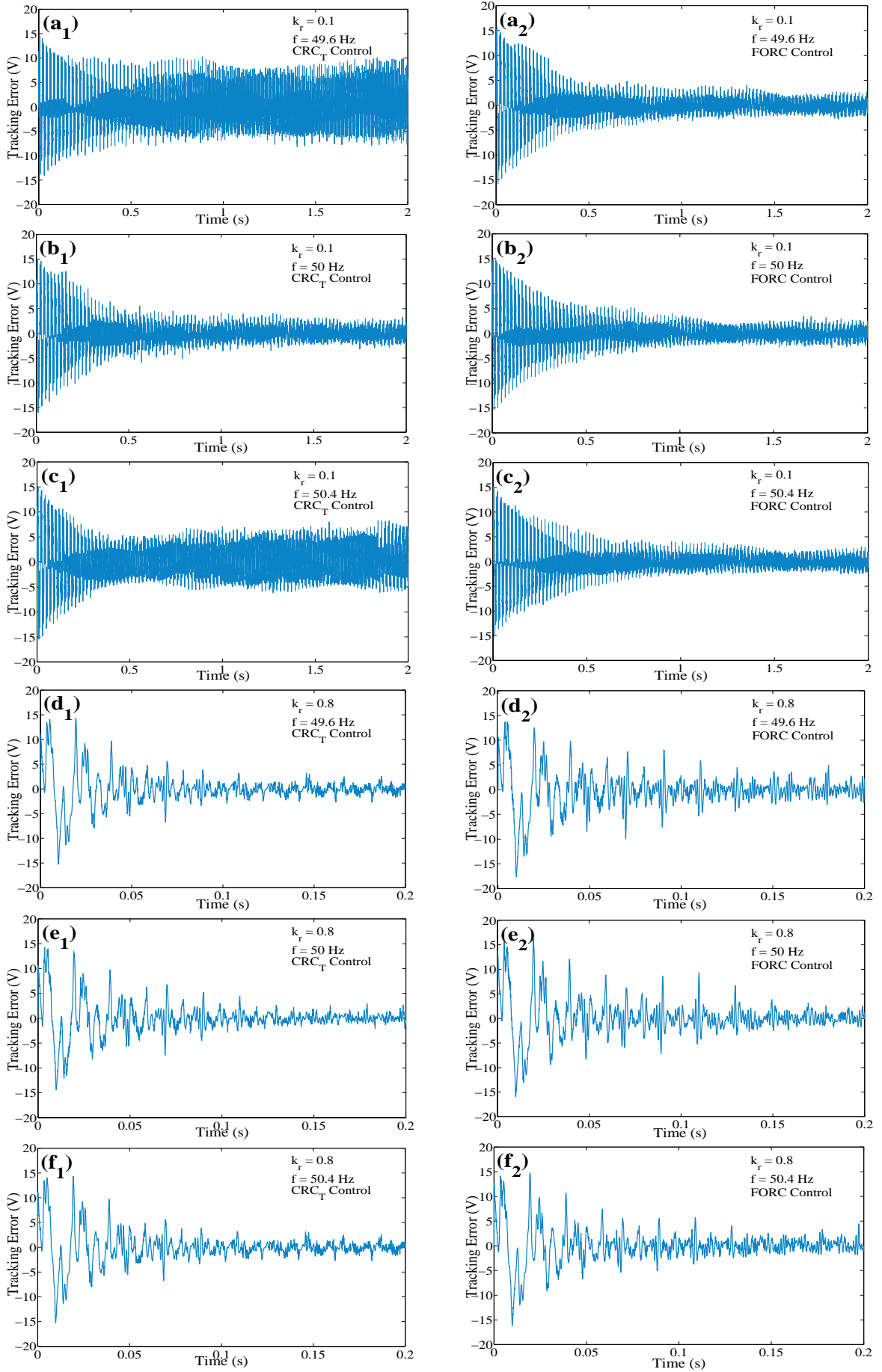


Figure 4.10: Transient error history with various k_r when $f_s = 10$ kHz and $Q(z) = 0.25z^1 + 0.5 + 0.25z^{-1}$ (fundamental frequency peak voltage = 50 V).

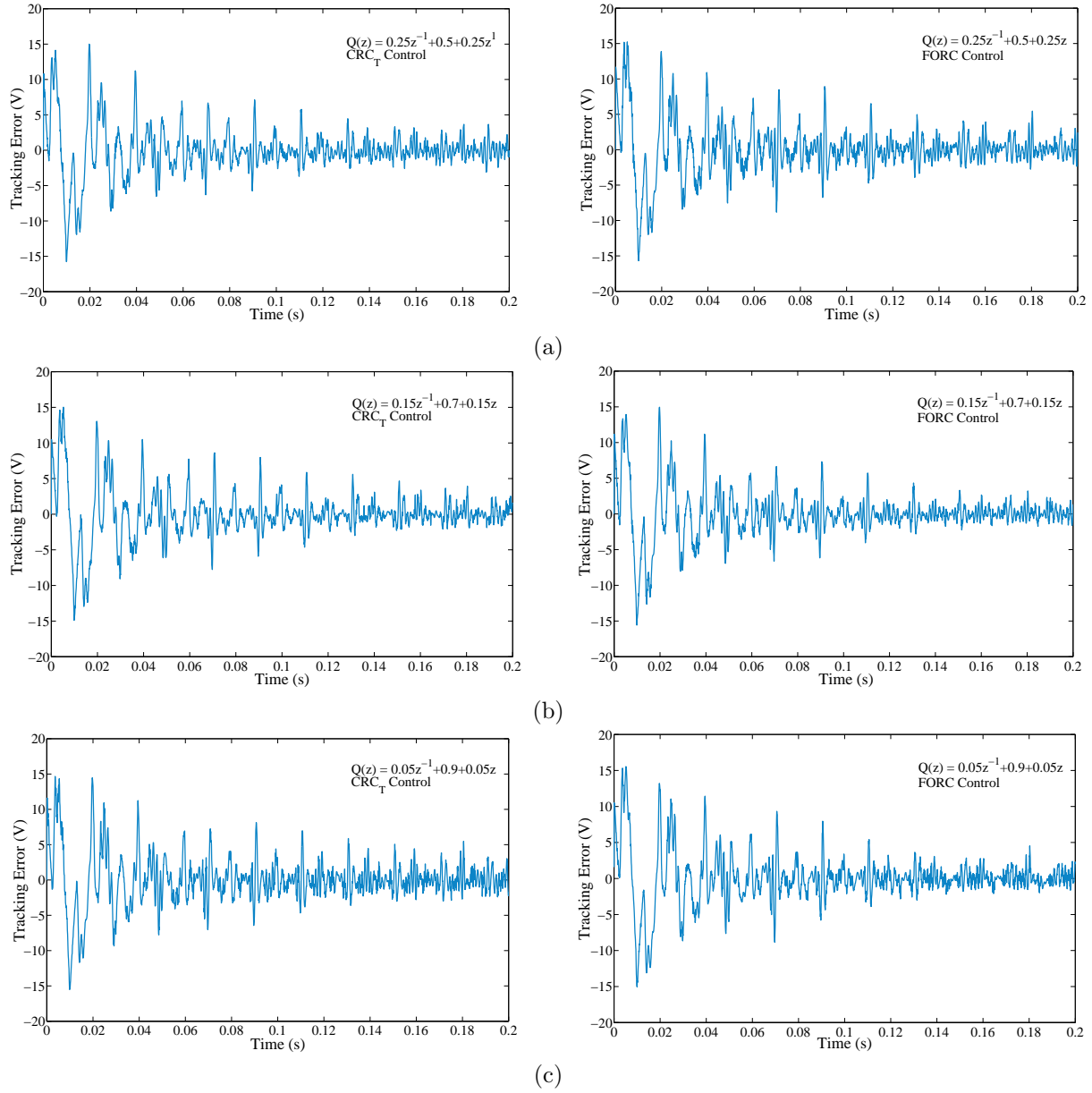


Figure 4.11: Transient responses for different $Q(z)$ with $k_r = 0.8$, $f = 49.6$ Hz and $f_s = 10$ kHz (fundamental frequency peak voltage = 50 V).

Table 4.4: Convergence time and steady-state error for various k_r .

k_r	$f(\text{Hz})$	CRC _T		FORC	
		Convergence time	Error (rms)	Convergence time	Error (rms)
0.1	49.6	1.2 sec	3.8 V	1.2 sec	1.3 V
	50	1.2 sec	1.2 V	1.2 sec	1.2 V
	50.4	1.2 sec	3.4 V	1.2 sec	1.3 V
0.8	49.6	0.13 sec	1.1 V	0.13 sec	0.7 V
	50	0.13 sec	0.8 V	0.13 sec	0.7 V
	50.4	0.13 sec	1.1 V	0.13 sec	0.7 V
1.2	49.6	0.12 sec	1.1 V	0.13 sec	0.7 V
	50	0.13 sec	0.8 V	0.12 sec	0.7 V
	50.4	0.13 sec	1.1 V	0.13 sec	0.6 V

further increasing the sampling frequency can reduce the tracking error and higher sampling rate might give performance nearly similar to the FORC performance. PWM converters are operated at switching frequencies less than 20 kHz and Figure 4.7 shows that if the sampling frequency for PWM converter is greater than 10 kHz CRC_T can still track a variable frequency reference signal with reasonably low steady-state error value. The FD filter based FORC at fixed sampling frequency is clearly capable of tracking/rejecting periodic signals of variable frequencies at all sampling frequencies and higher sampling leads to higher control accuracy.

Figure 4.8 shows the steady-state response of the output voltage $v_c(t)$ and the load current $i_o(t)$ of the CRC_T controlled single-phase inverter with different loads when $f = 49.6$ Hz and $f_s = 10$ kHz. The results indicate that CRC_T control offers low THD output voltage ($\approx 1.93\%$) under linear load and high THD output voltage ($\approx 4.98\%$) under rectifier load.

Figure 4.9 shows the steady-state response of the output voltage $v_c(t)$ and load current $i_o(t)$ of the FORC controlled inverter with different loads when $f = 49.6$ Hz and $f_s = 10$ kHz. The results indicate that FORC control offers very low THD ($\leq 2\%$) output voltage with both linear and non-linear loads.

Table 4.4 and Figure 4.10 show several typical examples of the transient responses of CRC_T and FORC with different k_r in the presence of frequency variations. It can be noticed that the convergence rate is proportional to the gain k_r for both CRC_T and FORC controllers, *i.e.* larger k_r leads to faster convergence rate. Furthermore, although the theoretical stability is in the region $k_r \in [0, 2]$, very small control gain, such as $k_r = 0.1$ yields excessive convergence time, and $k_r \geq 1.3$ would lead to system instability in experiments. In this case, $k_r \in [0.8, 1.2]$ for both CRC_T and FORC control schemes yields satisfactory convergence rate. The difference between the theoretical and experimental stability limits of k_r is due to uncertainties in practice, such as load disturbance, computation delay and parameter variations.

Figure 4.11 shows several typical examples of the transient responses of the tracking errors of CRC_T and FORC with $k_r = 0.8$ and three different $Q(z)$ in the presence of frequency variations. The experimental results show that, like CRC [45], FORC controllers with all the three $Q(z)$ produce almost the same transient and steady-state responses. The role of $Q(z)$ in FORC controller is to make a trade-off between system robustness and tracking accuracy [45]. $Q(z) = 0.25z^1 + 0.5 + 0.25z^{-1}$ usually provides sufficient bandwidth for FORC controllers to compensate harmonic distortion.

The experimental results shown in Figure 4.6 – 4.11 and Table 4.3 – 4.4 clearly show that the

FORC system is fully compatible with a CRC system, with much better performance in terms of steady-state error and THD. The experimental results also show that the control gain parameter k_r and low-pass filter $Q(z)$ behave in a very similar manner in both schemes. The proposed FD filter based FORC offers better control accuracy in the presence of frequency variations than CRC. Sampling frequency has a significant impact on the compensation accuracy of CRC but has moderate impact on that of the FORC.

4.5 CONCLUSION

This Chapter presents a systematic design and analysis approach of a FORC control scheme with fixed sampling rate to compensate periodic signals with variable frequency. A design enhancement has been suggested and stability criteria for the proposed FORC systems are derived. Comprehensive experimental results demonstrate that a well-designed FORC control system is fully compatible with a CRC system. It also shows that the sampling frequency does not have a significant impact on the tracking error performance of FORC controller in the presence of frequency variations, whereas CRC control performance is very sensitive to sampling frequencies.

Generally speaking, the proposed FORC method provides power converters with a simple, efficient and high performance real-time control solution for dealing with periodic signals of varying fundamental frequency. It can be used in many applications, such as the current control of grid connected converters, programmable AC power supply, active noise cancellation, and so on.

Chapter 5

TAYLOR SERIES EXPANSION BASED ADVANCED REPETITIVE CONTROLLER FOR POWER CONVERTERS

5.1 INTRODUCTION

Chapter 4 describes a Fractional Order Repetitive Control (FORC) scheme which is capable of working well under variable frequency reference signal conditions. However, a FORC controller needs to update its co-efficients every time the required fractional delay parameter changes. The Repetitive Control (RC) technique proposed in [49] for three-phase grid inverters uses the estimated grid frequency to adaptively update the RC period and resonant controller's resonant frequencies, while interpolation is used to preserve the RC rejection capability under non-integer samples per period. Wang *et al.* proposed a fractional delay based repetitive control scheme for single-phase PWM inverters, where a fractional delay low-pass filter is introduced to approximate the internal model of the fractional-period signals. Two different methods are introduced to design the Fractional Delay (FD) low-pass filters: the Lagrange interpolation method and least square method. Chen *et al.* have also proposed an improved RC control scheme with a Finite Impulse Response (FIR) filter [55]. A simple zero-crossing method has been used to detect the reference period of the variable grid frequency. This method performs well in low noise environments only. Finite impulse response FD filters have also been used in [79, 80] to realize the fractional part of the required non-integer delay. Another approach is to use a higher order repetitive controller to enhance the system robustness to reference frequency variations [98]. However, all of these techniques require the redesign of the FD filter coefficients with fractional delay variations. Redesigning and updating the FD filter coefficients during operation is not very feasible.

This Chapter presents a Taylor series expansion based digital repetitive controller designed to implement any (integer, non-integer) delay in the control of power converters occurring due to variations in the reference frequency. The Taylor series expansion transforms the fractional delay filter design problem to a differentiator/sub-filter design [99]. Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) FD filter concepts can be applied to realize the required fractional delay. This structure provides efficient on-line tuning capabilities *i.e.* the FD filter can easily generate any required fractional delay without redesigning the filter when the delay parameter varies. An example is used to show the effectiveness of this approach for a single-phase power inverter typical of single-phase grid-connected photo-voltaic systems. This Chapter provides a systematic approach for non-integer delay cases under a fixed sampling rate. This method designs an FD filter based on the well known Taylor series expansion, which realizes any required delay without redesigning the FD filter coefficients. Taylor series expansion based FD filters have been widely used in signal processing and circuit theory [91, 92, 100, 101]. Only few references have been cited here. The main contribution of this Chapter is the application of a Taylor series expansion based FD filter to modify the RC controller for control of power converters working under variable frequency reference signal conditions. The FORC requires

the redesign or recalculation and updation of the FD parameters online when the required delay parameter varies. This is quite a challenge to do. A Taylor series expansion based RC control seems to be an attractive choice as only one parameter needs to be calculated and updated in real time. However, the computational complexity of an FORC would be less than a Taylor series expansion based RC controller of same order.

This Chapter is organized as follows. Section 5.2 provides an insight into the Advanced Repetitive Control (ARC) scheme. Section 5.3 presents the experimental investigation of the proposed control, and finally the conclusion is given in Section 5.4.

5.2 TAYLOR SERIES EXPANSION BASED RC CONTROLLER

5.2.1 Design

Any fractional delay can be approximated using a Taylor series expansion. It uses various sub-filters to approximate the required fractional delay. Assuming that $z^{-N_o} = z^{-(N_i+F)}$ where $N_i = \text{int}[N_o]$ is the integer part of N_o and $F = N_o - N_i, 0 \leq F < 1$ is the fractional part. The fractional delay $z^{-F} = e^{-jwF}$ can be expressed as a polynomial in F using the Taylor series expansion as follows [102–104]:

$$e^{-jwF} = \sum_{k=0}^{\infty} \frac{(-F)^k}{k!} (jw)^k \quad (5.1)$$

Since the fractional part is small *i.e.* $F < 1$, the term F^{M+1} and other higher order multiples of F approaches zero when M is large. Therefore (5.1) can be approximated as:

$$e^{-jwF} \approx \sum_{k=0}^M \frac{(-jw)^k}{k!} F^k \quad (5.2)$$

where M is the order of the polynomial,

$$e^{-jwF} \approx \sum_{k=0}^M P_k(z) F^k \quad (5.3)$$

where $P_k(z) = (-jw)^k/k!$ is the scaled frequency response of k^{th} order differentiator [99].

The FD filter response approaches its ideal behavior as the value of M approaches infinity. According to (5.3) the FD filter can be implemented by $M + 1$ different sub-filters $P_k(z)$ where $k = 0, 1 \dots M$ as shown in Figure 5.1. This structure has been referred as a Farrow structure in [104–106].

Many techniques are available in the literature to design these sub-filters [94, 104–108]: IIR and FIR sub-filters can be employed [92, 94, 109]. Once the $M + 1$ sub-filters ($P_k(z)$) are designed and inserted into the structure of Figure 5.1, only the parameter F needs to be adjusted to achieve any fractional delay. The sub-filters parameters remain unchanged even in the case of fractional delay variations.

Simplest of all, Lagrange interpolation can be used to design $P_k(z)$ in the time-domain. This method is utilized here to design $M + 1$ sub-filters.

All the $M + 1$ sub-filters can be expressed as N^{th} order polynomials with constant coefficients and $N \geq M$ [110]. Usually $N = M$ is used. The Lagrange interpolation based sub-filter coefficients

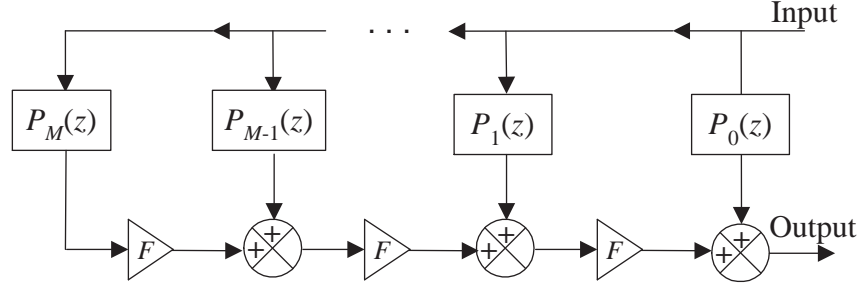


Figure 5.1: Taylor series expansion based FD filter.

can be calculated as follow:

$$\begin{aligned}
 C_t &= U_t^{-1} z_t \\
 \text{where } C_t &= [P_0(z) \ P_1(z) \ P_2(z) \ \dots \ P_M(z)]^T \\
 z_t &= [1 \ z^{-1} \ z^{-2} \ \dots \ z^{-M}]^T \\
 U_t &= \begin{bmatrix} 0^0 & 0^1 & 0^2 & \dots & 0^N \\ 1^0 & 1^1 & 1^2 & \dots & 1^N \\ 2^0 & 2^1 & 2^2 & \dots & 2^N \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ M^0 & M^1 & M^2 & \dots & M^N \end{bmatrix}
 \end{aligned} \tag{5.4}$$

For a third order Taylor series expansion based FD filter, $P_0(z) = 1$, $P_1(z) = -(11/6) + 3z^{-1} - (3/2)z^{-2} + (1/3)z^{-3}$, $P_2(z) = 1 - (5/2)z^{-1} + 2z^{-2} - (1/2)z^{-3}$, $P_3(z) = -(1/6) + (1/2)z^{-1} - (1/2)z^{-2} + (1/6)z^{-3}$ are obtained when $N = M$. Generally, a first order FD filter is sufficient in most applications although a higher order FD filter can further reduce error. For higher order FD filter implementations, optimizing a FD filter using the method described in Section 4.3.1 can lead to better approximation and less error if the higher frequency harmonics contribute significantly to the error. If the steady-state error is dominated by the low frequency harmonics, a non-optimal FD filter may also perform well. The transfer function of the FD filter ($G_t(z)$), shown in Figure 5.1, is:

$$G_t(z) = \sum_{k=0}^M P_k(z) F^k \tag{5.5}$$

Section 2.3.2 describes the basic plug-in repetitive control system as shown in Figure 5.2. The overall structure of an RC controlled system remains unchanged. However the internal structure of the RC ($G_{rc}(z)$) is modified to include a Taylor series expansion based FD filter ($G_t(z)$) and the new RC structure is referred as Advanced Repetitive Controller (ARC) and is represented by $G_{rt}(z)$.

$$G_{rt}(z) = k_r \frac{G_t(z) z^{-N_i} Q(z)}{1 - G_t(z) z^{-N_i} Q(z)} G_c(z) \tag{5.6}$$

The advanced repetitive controller is displayed in Figure 5.3. The full delay is implemented with the integer delay z^{-N_i} and the fractional delay filter $G_t(z)$. The ARC controller can be plugged-into a conventional feedback controlled plant, *i.e.* in Figure 5.2 $G_{rc}(z)$ can be replaced by this ARC structure shown in Figure 5.3. The transfer function from $y_{ref}(z)$ and $d(z)$ to $y(z)$

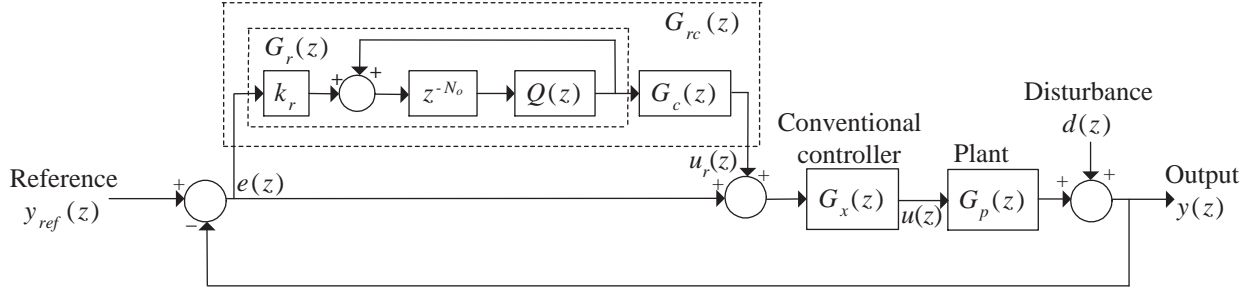


Figure 5.2: Block diagram of discrete time RC control system.

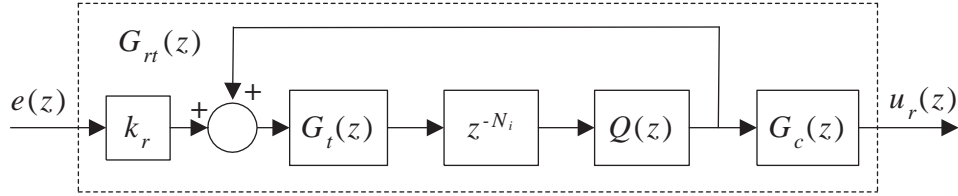


Figure 5.3: The Taylor series expansion based advanced repetitive control structure.

(Figure 5.2) with plugged-in ARC $G_{rt}(z)$ is given by:

$$\frac{y(z)}{y_{ref}(z)} = \frac{(1 + G_{rt}(z))G_x(z)G_p(z)}{1 + (1 + G_{rt}(z))G_x(z)G_p(z)} = \frac{(1 - G_t(z)z^{-N_i}(1 - k_r G_c(z)))H(z)}{1 - G_t(z)z^{-N_i}(1 - k_r G_c(z)H(z))} \quad (5.7)$$

$$\frac{y(z)}{d(z)} = \frac{1}{1 + G_x(z)G_p(z)} (1 - G_t(z)z^{-N_i}) \times \frac{1}{1 - G_t(z)z^{-N_i}(1 - k_r G_c(z)H(z))} \quad (5.8)$$

where $H(z)$ is given by:

$$H(z) = \frac{G_x(z)G_p(z)}{1 + G_x(z)G_p(z)} \quad (5.9)$$

From (5.5), (5.6), (5.7), (5.8) and (5.9) the closed-loop ARC system stability can be guaranteed if the following conditions hold:

- The roots of $1 + G_x(z)G_p(z) = 0$ are inside the unit circle.
- The roots of $1 - G_t(z)z^{-N_o}(1 - k_r G_c(z)H(z))$ are also in the stable region *i.e.* inside unit circle. Hence,

$$\|G_t(z)(1 - k_r G_c(z)H(z))\| < 1, \forall z = e^{j\omega}, \quad 0 \leq \omega \leq \pi/T \quad (5.10)$$

The bandwidth of $G_t(z)$ is greater than the bandwidth of the low-pass filter $Q(z)$ then $|G_t(z)| = 1$ in the pass-band of $Q(z)$. Therefore, the stability criteria of ARC is similar to the stability criteria for conventional repetitive controllers.

The magnitude response of a first order Taylor series expansion based FD filter $G_t(z)$ using Lagrange interpolation is given in Figure 5.4 for a fractional delay range 0:0.1:0.9. It indicates that the filter is capable of fractional delay estimation in the low frequency band up to nearly 50% of the Nyquist frequency; which is suitable for the control of PWM converters.

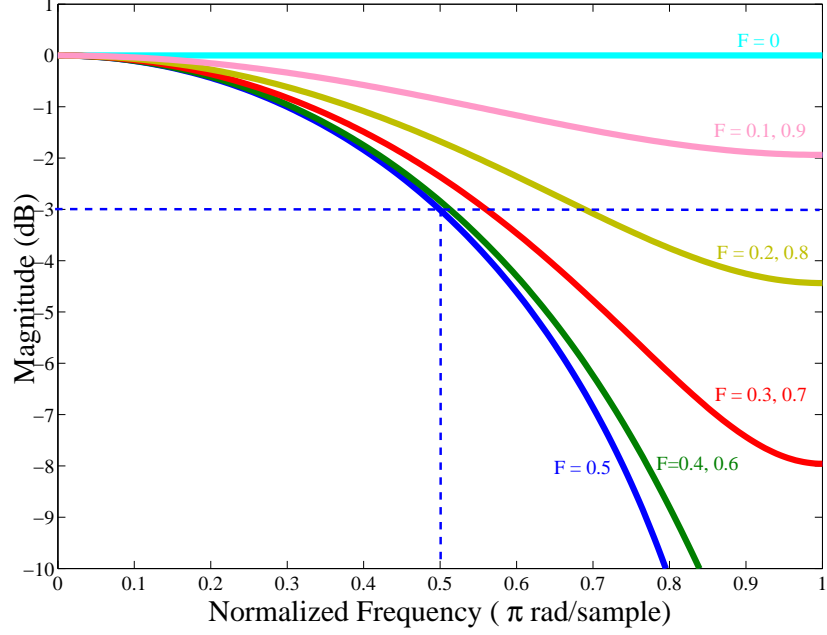


Figure 5.4: The magnitude response of a first-order Taylor series expansion based FD filter $G_t(z)$.

5.2.2 Performance Analysis

The design procedure for the Taylor series expansion based fractional delay filter can be summarized as follow:

- For a Taylor series expansion based RC filter implementation, select the order M of the FD filter.
- For FIR Lagrange interpolation based sub-filter implementation, select the order N of the polynomial.
- Calculate the sub-filter coefficients using (5.4).
- Measure the real frequency of the reference signal f and calculate the total desired delay $N_o = f_s/f$.
- Calculate fractional delay $F = N_o - N_i$ where $N_i = \text{int}[N_o]$.

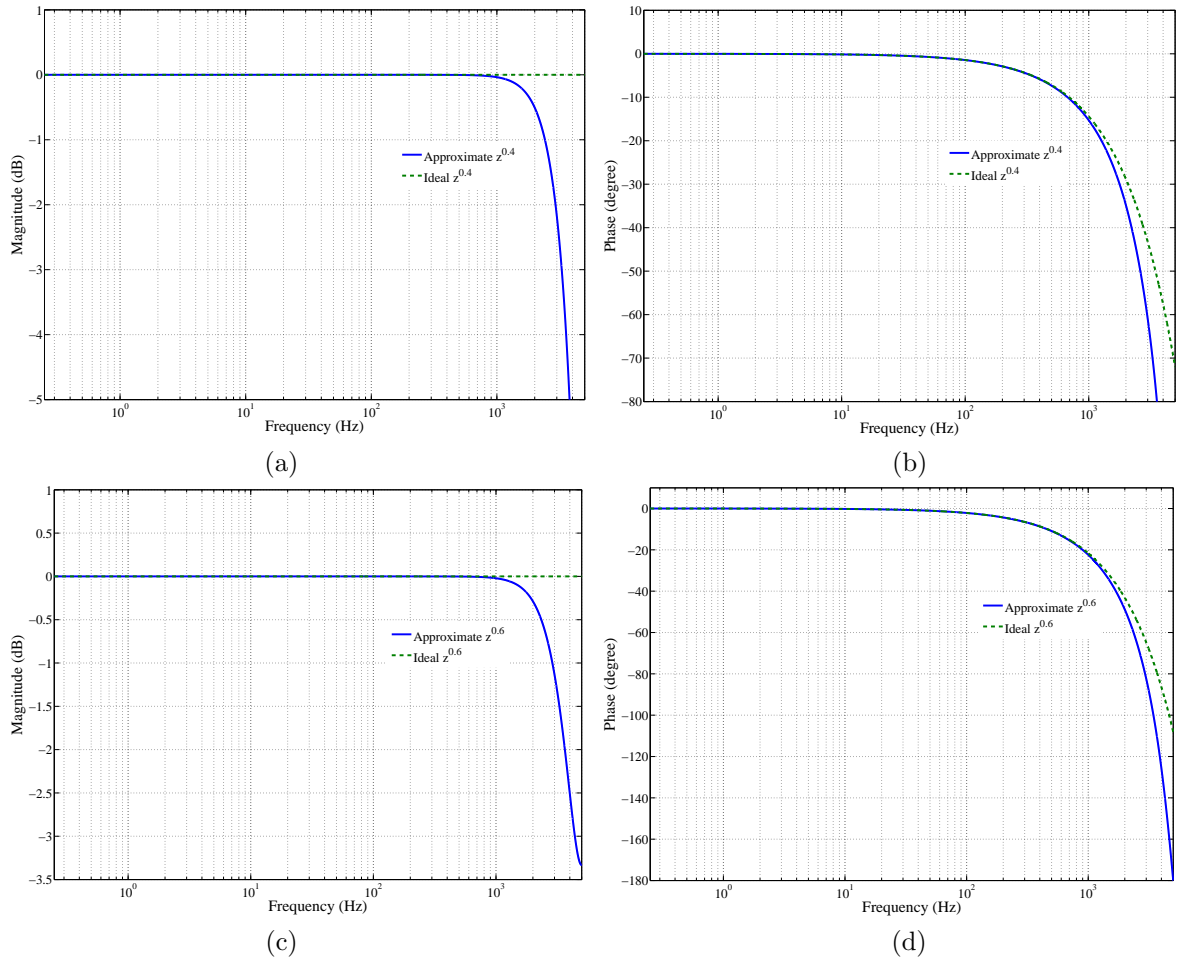
Two fractional delay filters $G_{t1}(z)$ and $G_{t2}(z)$ are designed for two different fundamental frequencies, 49.9 Hz and 50.1 Hz respectively. Table 5.1 lists the parameters of both filters.

Figure 5.5 shows the frequency response of the Taylor series expansion based fractional delay parts and the ideal non-integer delays. Both the magnitude and the phase response show close approximation to ideal behavior at low frequencies. Therefore, it can be concluded that the designed filters perform well in low frequency band *i.e* 50% of the Nyquist frequency.

Bode plots of the ARC at 49.9 Hz and 50.1 Hz are given in Figure 5.6 and are represented by $G_{t1}(z)$ and $G_{t2}(z)$ respectively. This figure also contains a Bode plot of Conventional Repetitive Control (CRC) at both frequencies. The CRC parameters at both of these frequencies are exactly the same and hence the Bode plots. z^{-200} represents the Bode plot of the CRC. The low-pass filter $Q(z) = 0.25z^1 + 0.5 + 0.25z^{-1}$ is used in CRC and ARC controllers. To clearly demonstrate the harmonic frequencies, certain parts of the Bode plot are focused in part (b) and (c). In Figure 5.6 (b), when the reference frequency varies ($\Delta f = \pm 0.1$) from its nominal value

Table 5.1: Taylor series expansion based FD filter parameters.

	$G_{t1}(z)$	$G_{t2}(z)$
Fundamental frequency (f)	49.9 Hz	50.1 Hz
Sampling frequency (f_s)	10 kHz	
Filter order (M)	2	
Sub-filters' polynomial degree (N)	2	
Total delay (N_o)	200.4	199.6
Fractional part (F)	0.4	0.6
Integer part (N_i)	200	199
Sub-filter $P_0(z)$	1	
Sub-filter $P_1(z)$	$-1.5 + 2z^{-1} - 0.5z^{-2}$	
Sub-filter $P_2(z)$	$0.5 - 1z^{-1} + 0.5z^{-2}$	

Figure 5.5: Comparison of frequency responses (a) $z^{0.4}$ Magnitude approximation (b) $z^{0.4}$ Phase approximation (c) $z^{0.6}$ Magnitude approximation (d) $z^{0.6}$ Phase approximation.

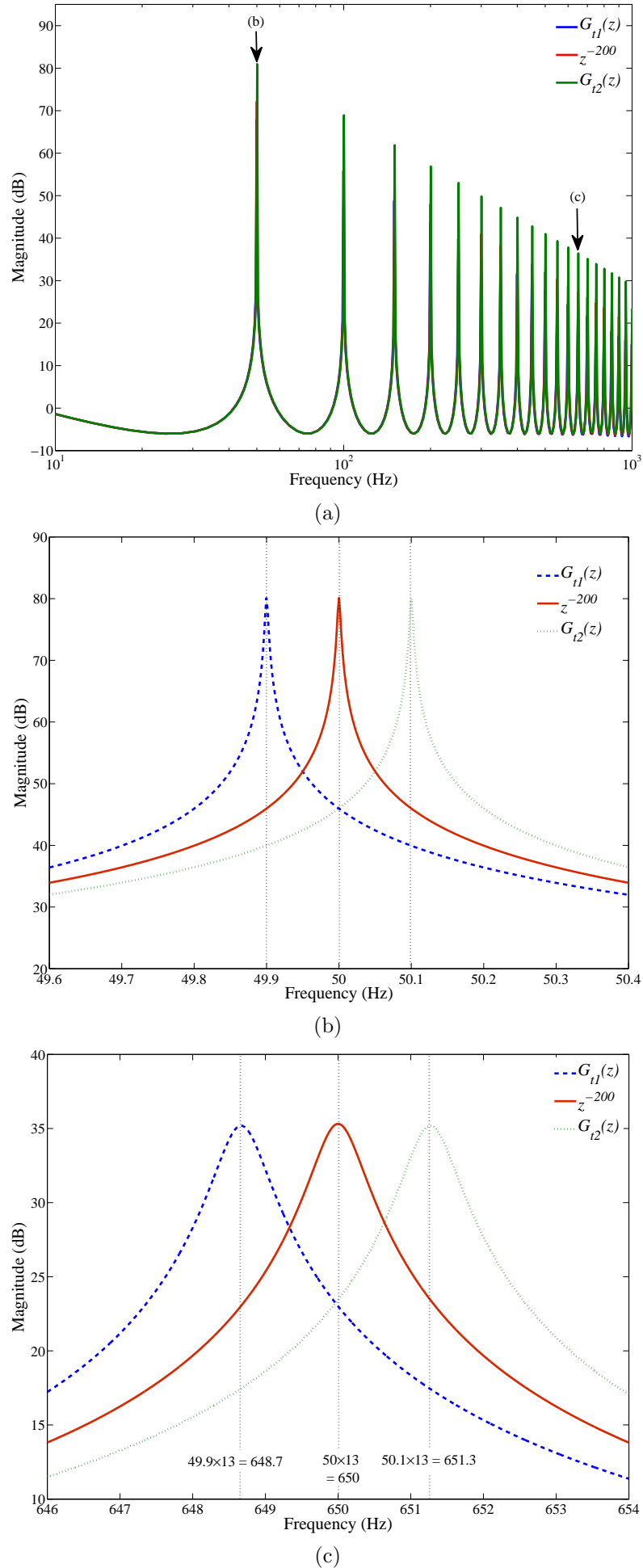


Figure 5.6: Magnitude response of the ARC: (a) within a frequency range of 10 Hz to 1 kHz (b) fundamental frequency component (c) 13th harmonic.

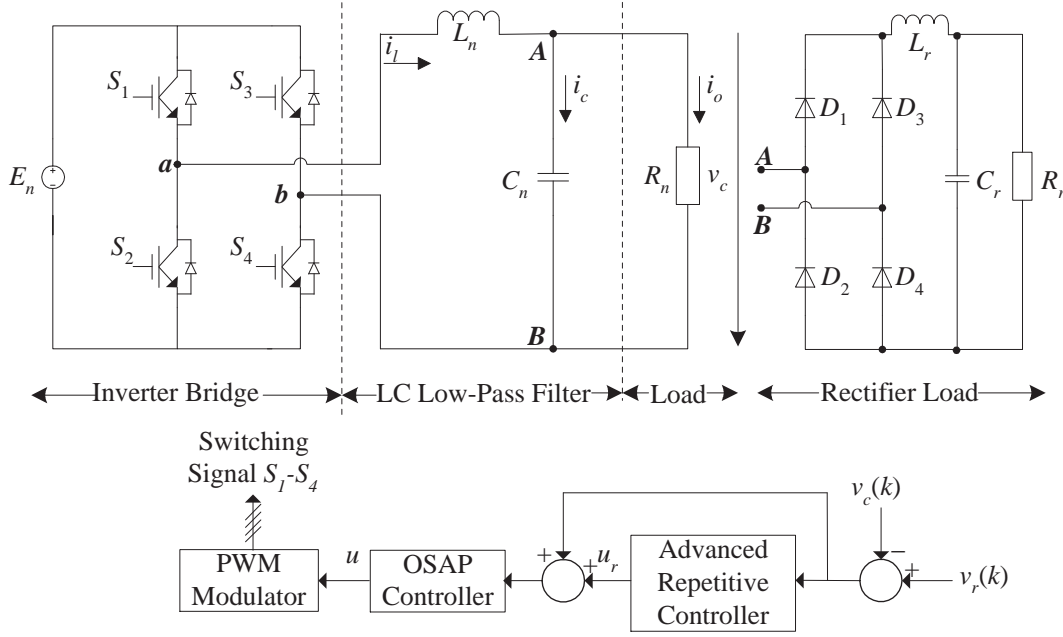


Figure 5.7: An ARC controlled single-phase PWM inverter.

the corresponding magnitude of conventional RC decreases quickly at fundamental frequency ($f = 50 \pm 0.1$). However, the ARC brings the resonant peaks at the desired fundamental and harmonic frequencies as represented by Figure 5.6 (b) - (c).

5.3 EXPERIMENTAL VALIDATION

5.3.1 System Setup

The proposed ARC scheme is validated by application to a single-phase inverter supplying a non-linear rectifier load as shown in Figure 5.7. This inverter system has already been used in Chapter 4 as an application of FORC control. Therefore the modeling of the inverter obtained in Chapter 4 is valid here as well. A One Sampling Ahead Preview (OSAP) controller is used as a conventional controller. This controller stabilizes the plant over a wide range of frequencies whereas the ARC is used to eliminate the steady-state error and minimize total harmonic distortion when the reference signal to be tracked is a variable frequency signal.

The control objective is to force the output voltage $y(k) = v_c(k)$ to precisely track the variable frequency reference signal $y_{ref}(k) = v_r(k)$. The inverter and control system parameters are given in Table 5.2.

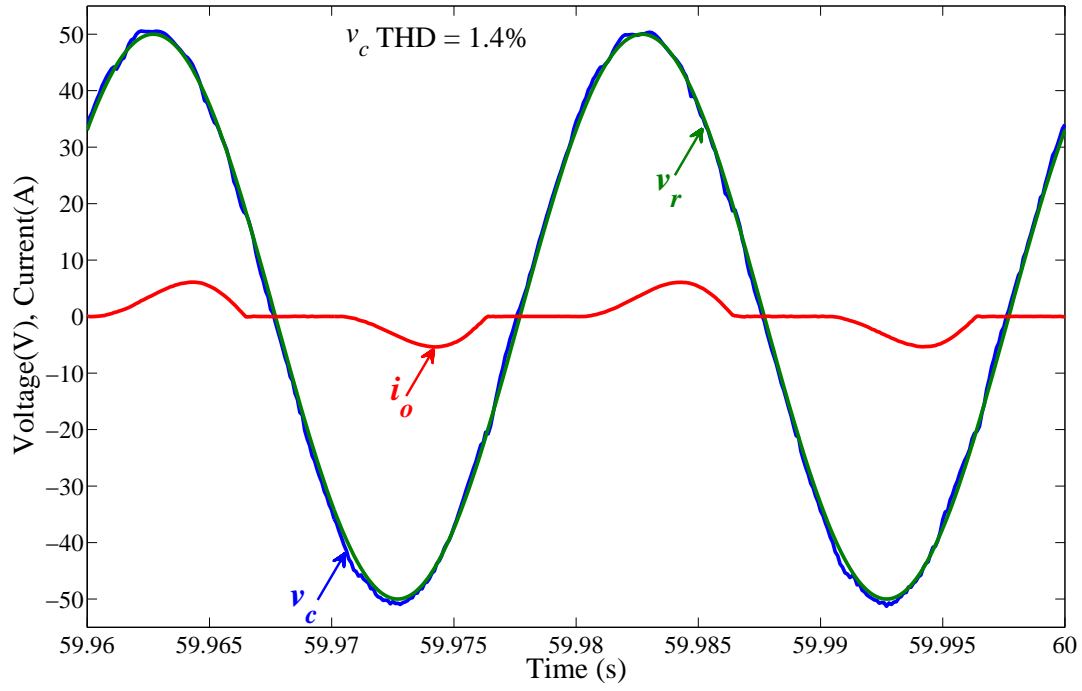
5.3.2 Results and Discussion

The transient response of the output voltage tracking error and steady-state response of the ARC controlled single-phase inverter, supplying a rectifier load at a nominal frequency ($f = 50\text{Hz}$) is shown in Figure 5.8.

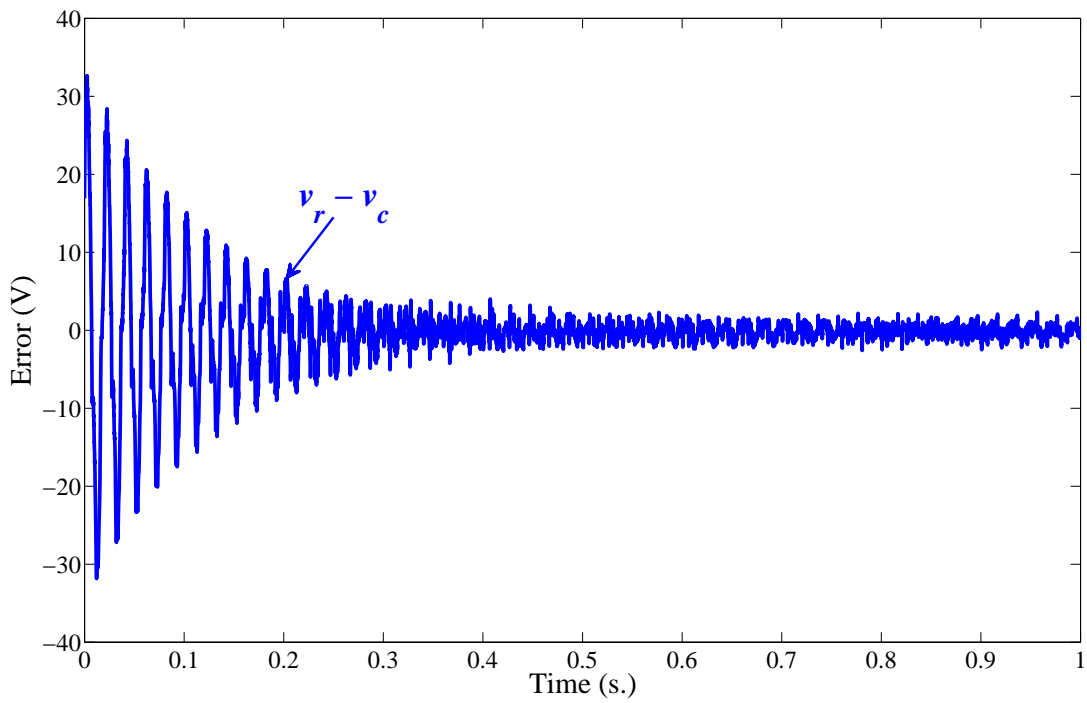
It can be seen that the output voltage (v_c) is a smooth sinusoid with THD = 1.4% and steady-state error is $\approx 1\text{V(rms)}$, which indicates that the control parameters are tuned properly for this experiment. Each experiment has been run for sixty seconds so that both the transient and steady-state response could be achieved. For a nominal frequency reference signal the required fractional delay is zero and the ARC acts exactly similar to a CRC controller.

Table 5.2: Inverter and control system parameters.

System setup		
Input voltage	E_n	100 V
Output ac voltage (peak)	v_c	50 V
Nominal frequency (fundamental)	f	50 Hz
Sampling frequency	f_s	10 kHz
Switching frequency	f_{sw}	10 kHz
Fundamental frequency range	Δf	1 Hz
Low-pass filter inductance	L_n	5 mH
Low-pass filter capacitance	C_n	30 μ F
Non-linear load inductance	L_r	5 mH
Non-linear load capacitance	C_r	1100 μ F
Non-linear load resistance	R_r	20 Ω
Controller parameters		
RC control gain	k_r	0.1
FD filter order	M	1
Sub-filter	$P_0(z)$	1
Sub-filter	$P_1(z)$	$-1 + z^{-1}$
Low-pass filter	$Q(z)$	$0.25z^{-1} + 0.5 + 0.25z^1$
Compensator	$G_c(z)$	z^3



(a) Steady-state response.



(b) Transient response of voltage tracking error.

Figure 5.8: An ARC controlled single-phase inverter response at nominal frequency $f = 50$ Hz.

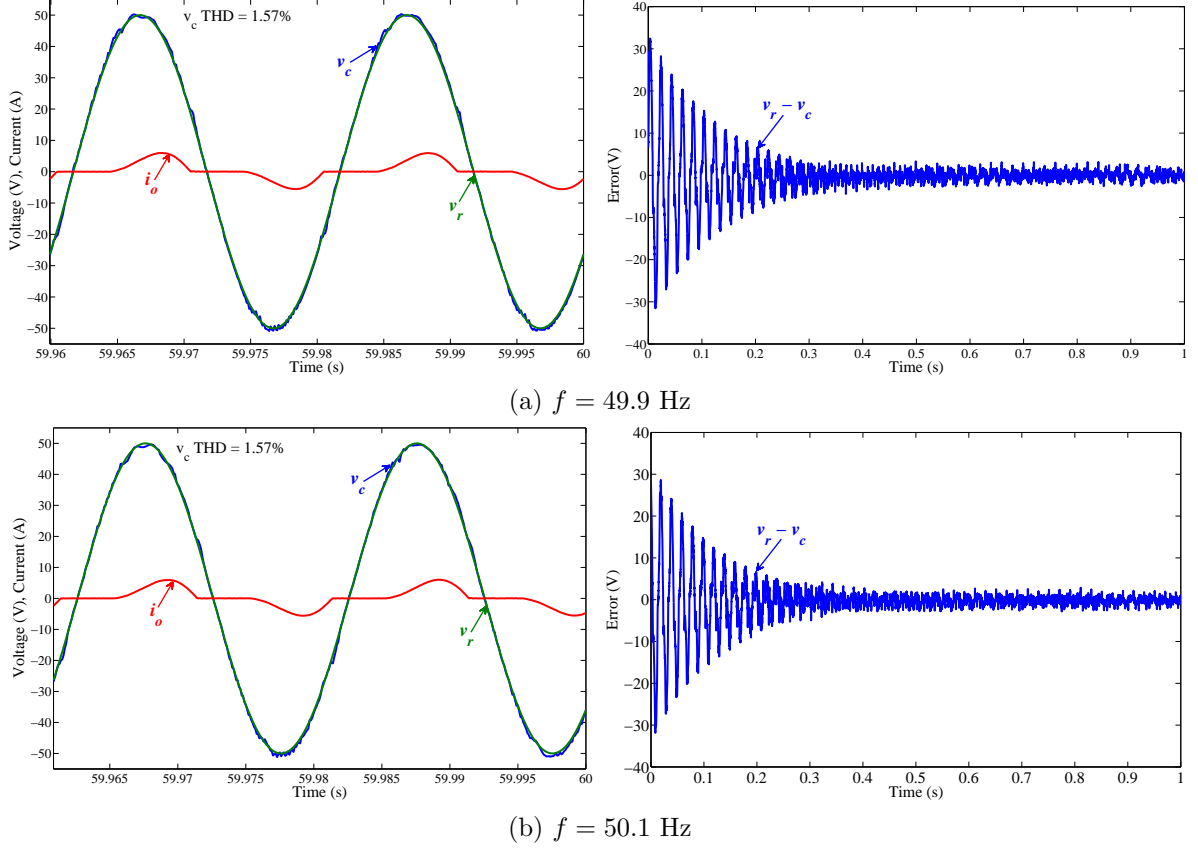


Figure 5.9: Steady-state response of ARC scheme at fundamental frequency $f = 50 \pm 0.1$ Hz.

Figure 5.9 and 5.10 show the steady-state response of the inverter output voltage and current at $f = 49.1$ Hz and $f = 50.1$ Hz using the ARC and CRC scheme respectively. Figure 5.9 shows that the THD of the output voltage of an ARC controlled inverter is 1.57% only, when the frequency of the reference signal is 49.1 Hz or 50.1 Hz. Both of these frequencies result in non-integer N_o . The steady-state error voltage is ≈ 1.5 V (peak). The error convergence time is ≈ 0.3 s. Thus ARC control scheme works well even when the frequency of the reference signal results in non-integer ratio N_o . However, the CRC control scheme in Figure 5.10 is clearly unable to track the reference signal as the THD of the output voltage and steady-state error values are very high. The THD of the output voltage is 4.42% and 6.50% at 49.1 Hz and 50.1 Hz respectively. The steady-state error at both frequencies is ≈ 5 V (peak).

When the fundamental frequency varies from its nominal value, the ratio of the sampling and reference frequency (N_o) may no longer be an integer. In the proposed control scheme, Taylor series expansion based fractional delay filter is used to realize the fractional delay. However, in CRC N_o is rounded off to the nearest integer, which results in shifting of the fundamental and harmonic frequency components from their actual values and hence the CRC performance degrades drastically.

Figure 5.11 shows the THD of CRC, ARC and FORC control approaches, when the frequency of the reference signal varies from 50 Hz to 50 ± 1 Hz. The FORC controller utilizes Lagrange interpolation based FD filter along with the CRC. It is clear from the Figure 5.11 that THD of CRC controlled inverter is highly fluctuating and it increases as N_o shifts away from integer values. The CRC still provides low THD values but only when the N_o is close to integer. However, the Taylor series based RC and FORC control schemes provide almost constant THD in the presence of frequency variations. Although the performance of FORC and ARC is almost same, constant FD filter parameters irrespective of the fractional delay value is a valuable asset

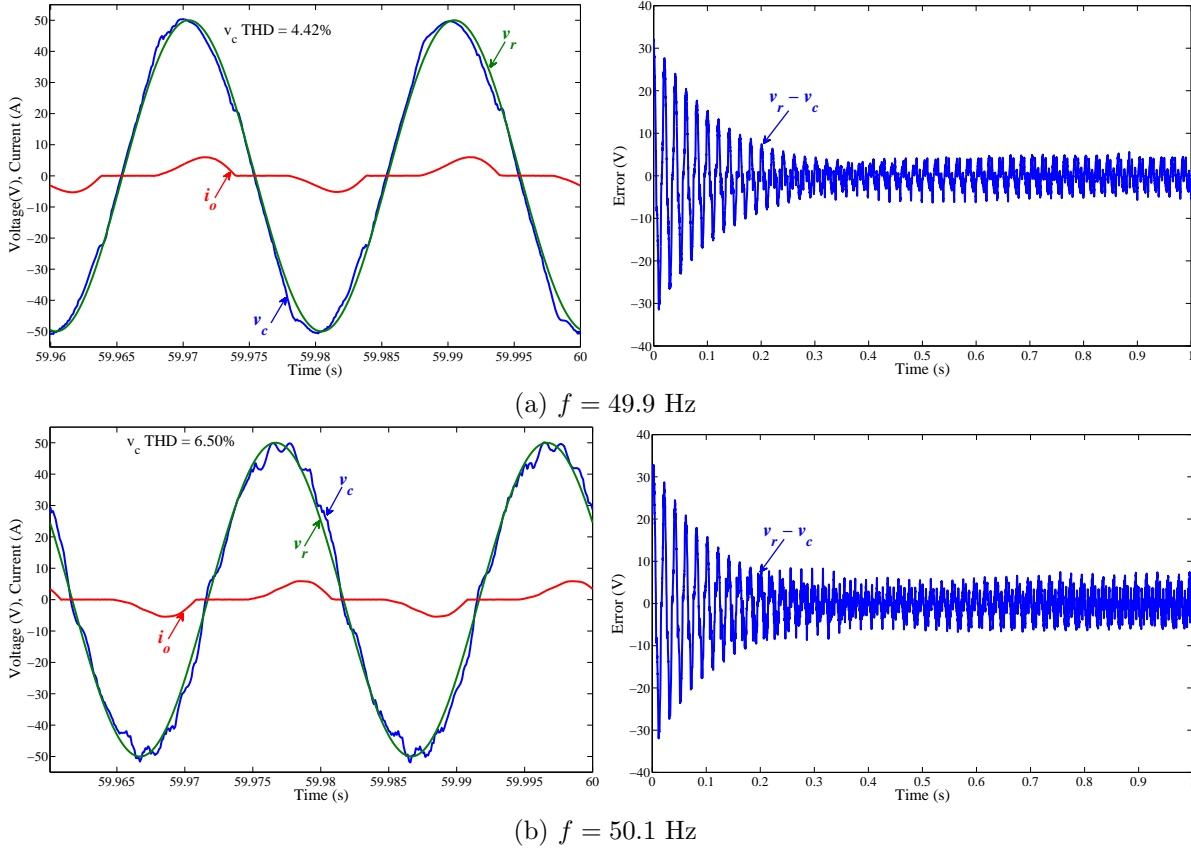


Figure 5.10: Steady-state response of conventional RC scheme at fundamental frequency $f = 50 \pm 0.1$.

of the latter scheme. It has already been shown in [79, 111] how the coefficients of FORC control varies by varying the required fractional delay.

5.4 CONCLUSION

A frequency adaptive repetitive control scheme is implemented for a single-phase power inverter typical of what is used for small scale grid-connected photo-voltaic systems. Taylor series expansion based fractional delay filter design is utilized to approximate the fractional delay. M^{th} order Taylor series expansion of the fractional delay results in the Farrow structure containing $M + 1$ sub-filters. Lagrange interpolation is used to design these sub-filters. Increasing the order M of the Taylor series expansion results in higher bandwidth. This control scheme performs really well within the bandwidth of the FD filter and tracks the variable frequency reference signal without redesigning the overall RC controller. Thus the stability conditions of the ARC controller remains same as that of CRC within the bandwidth of the FD filter. In an ARC controlled inverter the THD of the output signal remains almost constant and within acceptable limits during the reference signal frequency variations. The experimental results also show that the ARC controller tracks the variable frequency reference signal with nearly zero steady-state error.

The ARC control scheme is reconfigurable online, without redesigning the filter when the fractional delay parameter F varies. Effectiveness of the proposed scheme has been validated by the experimental results.

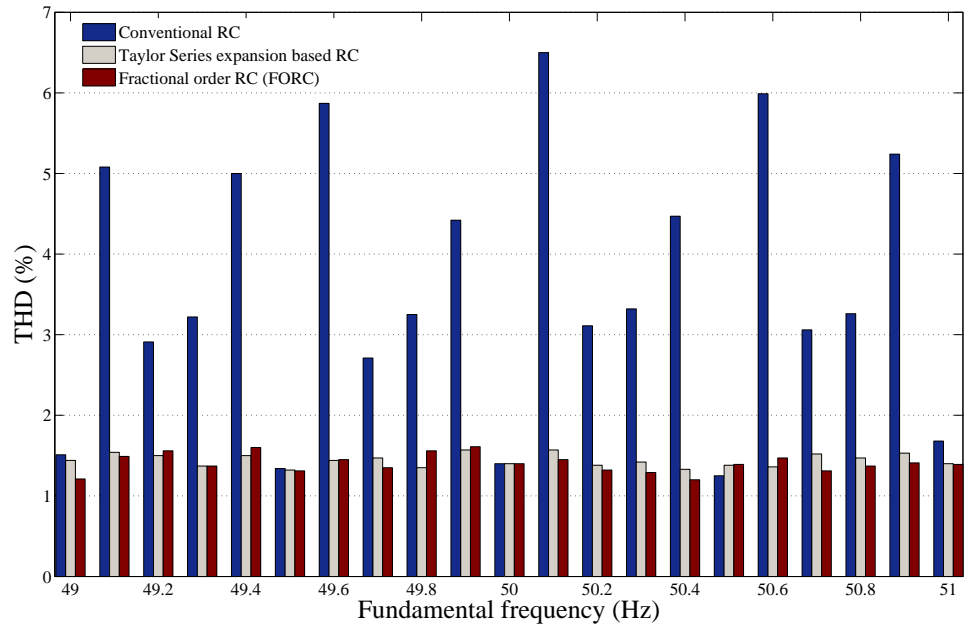


Figure 5.11: Comparison of output voltage (v_c) THD.

Chapter 6

ADVANCED REPETITIVE CONTROL OF GRID CONNECTED CONVERTERS

6.1 INTRODUCTION

Chapter 5 has described the design and analysis of an Advanced Repetitive Controller (ARC), which is a Taylor series expansion based digital repetitive controller. The ARC uses a Taylor series expansion based digital filter to realize a variable fractional delay. Chapter 5 has also presented the experimental results of an ARC controlled stand-alone single-phase inverter where the reference signal is considered to be the grid voltage signal which is a variable frequency signal. Practically, stand-alone inverters are not influenced by the frequency of a power system and the reference signal is a constant frequency constant voltage signal. However, the experiment described in Chapter 5 was performed to foresee and understand the performance of ARC under variable frequency environment.

In this chapter, an ARC controller is used to achieve a near unity power factor at the input of a three-phase PWM rectifier in the presence of varying frequency reference signal provided by the grid. The PWM rectifier considered here is a boost rectifier having a fixed steady-state voltage output and is connected to a grid of variable frequency. Modern electric devices are usually fed by diode or thyristor front-ends which are great sources of harmonics in the power system. To minimize grid harmonics either additional smart devices are used to get rid of existing harmonics or grid friendly devices (front-ends) are used which generate very limited harmonics. PWM rectifiers are the most commonly used grid friendly devices or front-ends which inject almost negligible harmonics to the grid and achieve nearly unity power factor.

This Chapter is organized as follow: Section 6.2 provides an overview of PWM rectifier operation and modelling. Section 6.3 explains the controller details. Section 6.4 presents the experimental results and suitability of the ARC control technique for grid connected converters, and finally the conclusion is given in Section 6.5.

6.2 PWM RECTIFIER

The use of PWM rectifiers in electrical power system has increased over the past few decades. PWM rectifiers allow bidirectional power flow and draw/supply nearly sinusoidal current from the grid. These attributes make PWM rectifiers a very obvious alternative to conventional diode rectifiers. There are two types of PWM rectifiers; current source output (buck) and voltage source output (boost) PWM rectifiers. The voltage source output PWM rectifiers, also known as boost rectifiers, operate to provide fixed dc voltage whereas the other one operates to provide a fixed current flow on the dc side. This Chapter is dedicated to the control of three-phase boost rectifiers connected to the grid. The main features of PWM rectifiers include [58, 112],

- Sinusoidal ac line current.

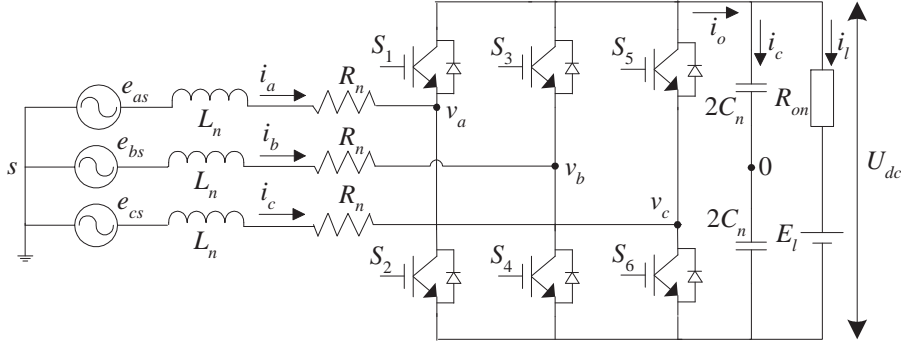


Figure 6.1: Circuit diagram of a three-phase boost rectifier.

- Low harmonic distortion of line current.
- Near unity power factor at the input of the rectifier.
- Stable and ripple free dc side output voltage or current.

6.2.1 Operation of PWM boost rectifier

Figure 6.1 shows a three-phase PWM rectifier. The three-phase line-neutral voltages are represented by e_{as} , e_{bs} , e_{cs} ; L_n and R_n represent ac-side inductor and equivalent series resistance of the ac-side inductor; C_n represents dc-side capacitor, R_{on} represents load resistance; $S_1 - S_6$ denote sinusoidal PWM signals, i_a , i_b , i_c denote ac-side line currents; U_{dc} denotes dc-bus voltage; E_l is the *emf* of the load; and i_o , i_c , i_l denote dc-bus current, capacitor current and load current respectively. It is assumed, that the three-phase ac voltages provided by the grid are balanced. Thus:

$$\begin{aligned} e_{as} &= E \sin(\omega t) \\ e_{bs} &= E \sin(\omega t - 120^\circ) \\ e_{cs} &= E \sin(\omega t + 120^\circ) \end{aligned} \quad (6.1)$$

$$\begin{aligned} i_a &= I \sin(\omega t + \Phi) \\ i_b &= I \sin(\omega t - 120^\circ + \Phi) \\ i_c &= I \sin(\omega t + 120^\circ + \Phi) \end{aligned} \quad (6.2)$$

where E , I and ω are peak voltage and current amplitudes and angular frequency respectively. Φ is the phase difference between three-phase input voltages and currents. The controlled operation of the PWM rectifier is implemented to force this phase difference (Φ) between input voltage and current to zero. For a three-phase balanced system,

$$i_a + i_b + i_c = 0 \quad (6.3)$$

(6.3) is also true for three wire unbalanced system. However, it may or may not be true for ac systems with four wires. On an instantaneous basis, line-line voltages at the input of rectifier

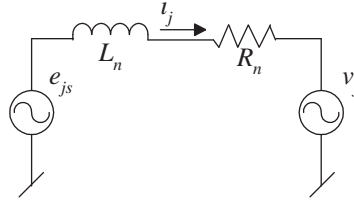


Figure 6.2: Single-phase representation of a rectifier.

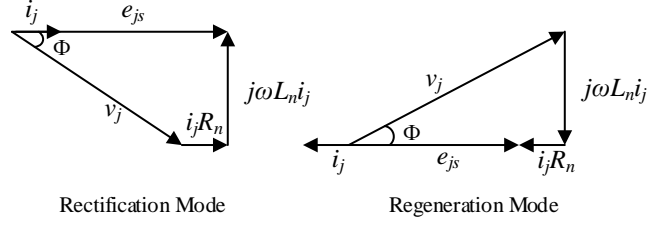


Figure 6.3: Phasor diagram of one phase of a three-phase rectifier operating in two (rectification and inversion) different modes at unity power factor.

are given as:

$$\begin{aligned}
 v_{ab} &= (S_a - S_b) \frac{U_{dc}}{2} \\
 v_{bc} &= (S_b - S_c) \frac{U_{dc}}{2} \\
 v_{ca} &= (S_c - S_a) \frac{U_{dc}}{2}
 \end{aligned} \tag{6.4}$$

where S_a , S_b and S_c are the switching functions of three legs of the rectifier. The value of switching function is +1 when the top switch is on and bottom switch is off, and -1 when bottom switch is on and top switch is off. The magnitude of the converter's input voltages v_j where $(j = a, b, c)$ depend upon the dc bus voltage and modulation index of the PWM signals. The ac side of the rectifier can be considered as two voltage sources (e_{js} and v_j), where $(j = a, b, c)$, connected through an inductor L_n having a series resistance R_n as shown in Figure 6.2. If the phase angle between the two sources is controlled, indirectly the magnitude and phase angle of the inductor current is controlled. Three-phase PWM rectifier has two operating modes [50, 113, 114]; rectification and regeneration mode.

Figure 6.3 shows the phasor diagram of one phase of the three-phase rectifier at unity power factor in both modes (rectification and inversion/regeneration) of operation [113]. In rectification mode power flows from ac-side to dc-side whereas power flow direction is reversed in regeneration mode. Thus:

- In rectification mode: Grid Power = Power loss + Converter side power.
- In regeneration mode: Converter side power = Power loss + Grid power.

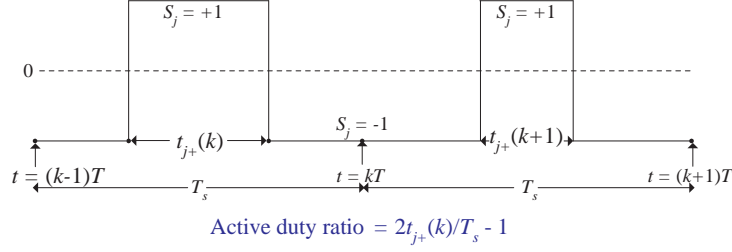


Figure 6.4: PWM switching waveform.

6.2.2 Mathematical modeling of PWM rectifier

Voltage equations on the input side of the Figure 6.1 can be written as:

$$\begin{aligned} e_{as} &= L_n \frac{di_a}{dt} + i_a R_n + v_a \\ e_{bs} &= L_n \frac{di_b}{dt} + i_b R_n + v_b \\ e_{cs} &= L_n \frac{di_c}{dt} + i_c R_n + v_c \end{aligned} \quad (6.5)$$

$$\begin{bmatrix} \dot{i}_a \\ \dot{i}_b \\ \dot{i}_c \end{bmatrix} = \begin{bmatrix} -\frac{R_n}{L_n} & 0 & 0 \\ 0 & -\frac{R_n}{L_n} & 0 \\ 0 & 0 & -\frac{R_n}{L_n} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} \frac{e_{as}-v_a}{L_n} \\ \frac{e_{bs}-v_b}{L_n} \\ \frac{e_{cs}-v_c}{L_n} \end{bmatrix} \quad (6.6)$$

$$\dot{U}_{dc} = -\frac{U_{dc}}{C_n R_n} + \frac{i_o}{C_n} + \frac{E_l}{R_n C_n}$$

The sampled-data form of (6.6) at time $t = (k+1)T_s$ is:

$$\begin{bmatrix} i_a(k+1) \\ i_b(k+1) \\ i_c(k+1) \end{bmatrix} = \begin{bmatrix} 1 - \frac{R_n T_s}{L_n} & 0 & 0 \\ 0 & 1 - \frac{R_n T_s}{L_n} & 0 \\ 0 & 0 & 1 - \frac{R_n T_s}{L_n} \end{bmatrix} \begin{bmatrix} i_a(k) \\ i_b(k) \\ i_c(k) \end{bmatrix} + \begin{bmatrix} \frac{e_{as}(k)T_s}{L_n} - \frac{U_{dc}}{2} \frac{d_a(k)}{L_n} \\ \frac{e_{bs}(k)T_s}{L_n} - \frac{U_{dc}}{2} \frac{d_b(k)}{L_n} \\ \frac{e_{cs}(k)T_s}{L_n} - \frac{U_{dc}}{2} \frac{d_c(k)}{L_n} \end{bmatrix} \quad (6.7)$$

Equation (6.7) can be regarded as three independent phase control sub-systems where T_s is the sampling period and $d_j(k)$ ($j = a, b, c$) is the active duty ratio of the respective switching function. The output equation can be given as:

$$y = \begin{bmatrix} i_a & i_b & i_c & U_{dc} \end{bmatrix}^T \quad (6.8)$$

On an instantaneous basis, the converter dc side current i_o can be written as:

$$i_o = \sum_{j=a,b,c} i_j S_j \quad (6.9)$$

As shown in Figure 6.4, each PWM switching waveform at port j , ($j = a, b, c$) is a pulse of magnitude +1 with width being $t_{j+}(k)$ in the sampling interval T_s and active duty ratio $d_j(k)$, ($j = a, b, c$) ($-1 \leq d_j(k) \leq 1$) being $d_j(k) = (t_{j+}(k) - (T_s - t_{j+}(k)))/T_s = (2t_{j+}(k))/T_s - 1$.

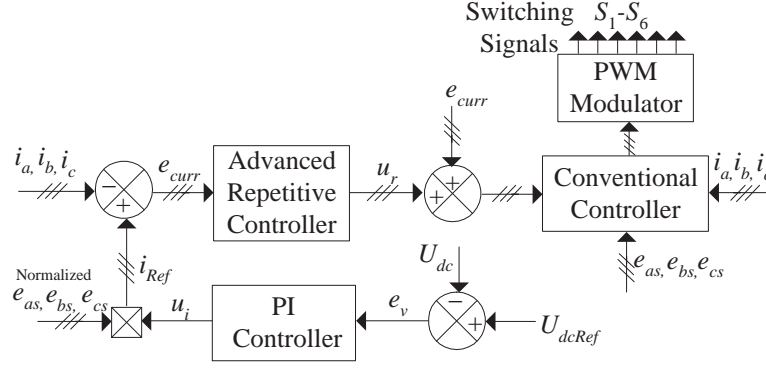


Figure 6.5: Three-phase PWM rectifier control scheme.

6.2.3 Minimum dc bus voltage requirement

The minimum dc link voltage obtained before the fully controlled operation of the rectifier is given by:

$$U_{dc/min} = \sqrt{3}v_{js}(peak) \quad (6.10)$$

This voltage is obtained as the diodes connected anti-parallel to all IGBT switches act as a three-phase diode bridge rectifier and charge the capacitor on dc side. If the IGBT switches are turned on/off before this condition is reached, the circuit would still be operating in an uncontrolled fashion. The boost nature of the rectifier can now be achieved by storing the energy in the inductor and releasing it. However higher dc bus voltages lead to higher switching losses.

6.3 CONTROL OF THREE-PHASE PWM CONVERTER

Control of the PWM converter is divided into two parts: output voltage control and input current control. A digital control scheme for both loops (voltage loop and current loop) is shown in Figure 6.5.

6.3.1 Output voltage control

Output voltage of the boost PWM rectifier is dc. Initially the PWM rectifier acts as a diode rectifier, due to the diodes connected anti-parallel to the IGBT switches, and charges the output capacitor to nearly the peak value of input phase to phase voltage. A PI controller is used to achieve a constant boosted dc output voltage. The transfer function of a discrete PI controller is given by:

$$= k_p + \frac{k_i T_s}{1 - z} \quad (6.11)$$

where k_p , k_i and T_s represent proportional gain, integral gain and sampling time respectively. The gains of the controller are designed to ensure stable and satisfactory dynamic operation of the system. The voltage loop control subsystem is shown in Figure 6.6.

From (6.9) and Figure 6.5 $i_o = i_a S_a + i_b S_b + i_c S_c = i_{peak}(\sin\Phi_1 S_a + \sin\Phi_2 S_b + \sin\Phi_3 S_c)$ [67], and the transfer function from i_o to i_{peak} can be written as [67]:

$$\frac{i_o}{i_{peak}} = \frac{k}{1 + 0.5T_s} \quad (6.12)$$

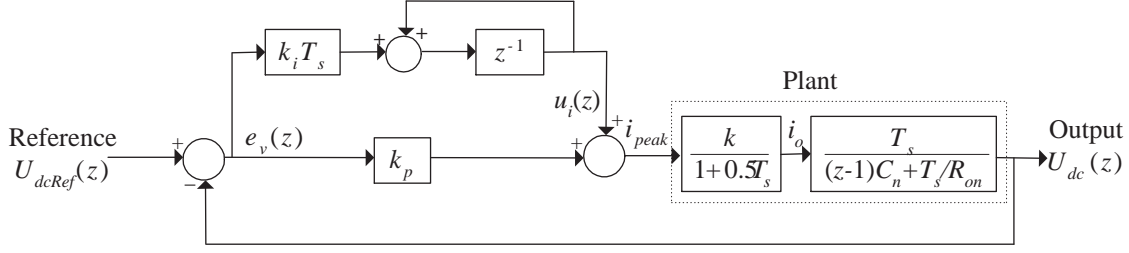


Figure 6.6: Voltage loop control.

where $-3 \leq k \leq 3$ and the transfer function from i_o to U_{dc} can be approximated as:

$$\frac{U_{dc}}{i_o} = \frac{T_s}{(z-1)C_n + T_s/R_{on}} \quad (6.13)$$

In the steady-state i_{peak} can be approximated as:

$$i_{peak} = \frac{2}{R_{on}} \frac{U_{dcRef}^2}{[e_{as} + e_{bs} + e_{cs}](peak)} = \frac{2}{R_{on}} \frac{U_{dcRef}^2}{3E} \quad (6.14)$$

Since $i_o = \frac{U_{dcRef}}{R_{on}}$ during steady-state, k can be calculated as:

$$k = \frac{U_{dcRef}}{i_{peak} R_{on}} \quad (6.15)$$

6.3.2 Input current control

The current controller for PWM rectifier is composed of two controllers: deadbeat and ARC controllers.

Deadbeat controller

Equation (6.7) can be treated as three single-phase subsystems and one phase subsystem is given as:

$$i_j(k+1) = \left(1 - \frac{R_n T_s}{L_n}\right) i_j(k) + \frac{e_{js}(k) T_s}{L_n} - \frac{U_{dc}}{2} \frac{d_j(k)}{L_n} \quad (6.16)$$

The nominal transfer function for each phase can be written as:

$$\frac{i_j(z)}{d_j(z)} = \frac{-U_{dc}}{2} \frac{T_s}{L_n z - L_n + R_n T_s} \quad (6.17)$$

For a deadbeat controller, also sometimes referred as predictive controller, the actual signal can track the reference signal with a delay of one sampling period T_s [37, 115]. Thus,

$$d_j(k) = \frac{2T_s}{U_{dc}(k)} \left[e_{js}(k) + \left(\frac{L_n}{T_s} - R_n \right) i_j(k) - \frac{L_n}{T_s} i_{jRef}(k) \right] \quad (6.18)$$

where $i_{jRef}(k) = i_j(k+1)$ and the transfer function of each phase current-loop control system (6.18) results in z^{-1} . Equation (6.18) is a deadbeat controller for a one phase sub-system.

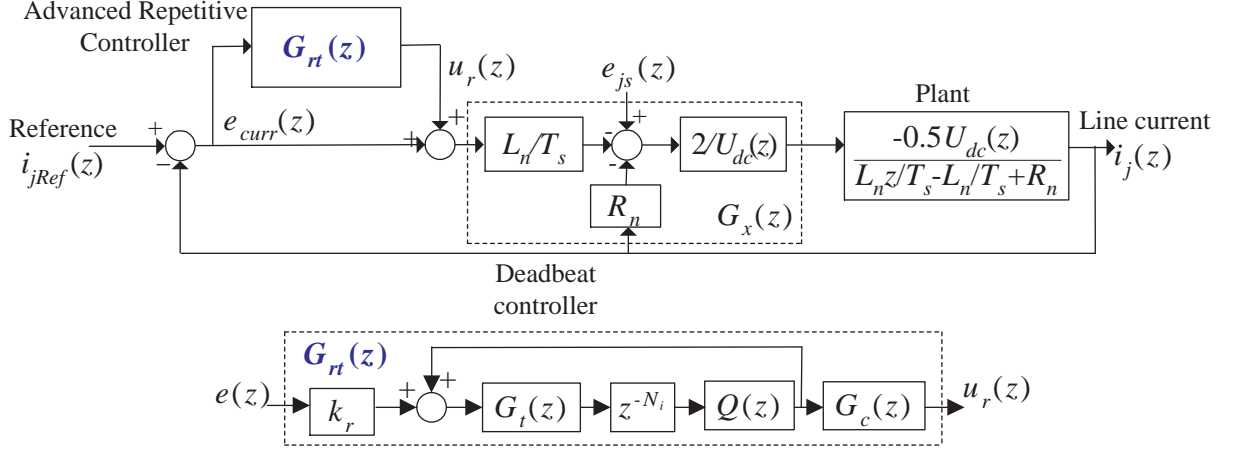


Figure 6.7: Current loop control.

Advanced repetitive controller

The design of ARC has been described in detail in Chapter 5. An ARC can be plugged in to a deadbeat controlled system. The over all current control loop is shown in Figure 6.7 where the ARC is represented by $G_{rt}(z)$. The $G_{rt}(z)$ is composed of fractional delay filter $G_t(z)$, delay line, low-pass filter $Q(z)$ and compensator $G_c(z)$. The $G_{rt}(z)$ is a Taylor series expansion based fractional delay filter (order = 2). The sub-filters in the fractional delay filter are also second order. The length of delay line z^{-N_i} varies depending upon the reference signal variations, as $N_i = f_s/f - F$ where f_s is the sampling frequency, f is the frequency of reference signal and F is the fractional delay value. $Q(z) = \alpha_1 z + \alpha_0 + \alpha_1 z^{-1}$ is a moving average low pass filter having $\alpha_1 = 0.25$ and $\alpha_0 = 0.5$. The compensator $G_c(z) = z^5$ has been selected¹. Other parameters of the three-phase grid connected rectifier system are given in Table 6.1. To verify the ARC scheme the input voltage of the converter in this experiment is set to very low voltage (30 V rms) level for safety purpose only. However, in case of practical grid converters this voltage is usually equal to the grid voltage and the control scheme performance, in terms of tracking of a signal, is independent of voltage and power levels of the converter.

6.4 EXPERIMENTAL RESULTS

A three-phase PWM rectifier connected to the grid has been controlled using ARC control technique. The experimental setup is shown in Figure 6.8. An AMETEK-MX bidirectional power supply was used to simulate a three-phase ac source *i.e.* grid. It could not be captured in the photograph of experimental setup shown in Figure 6.8.

The frequency f of the three-phase ac voltage is variable. The frequency of the input voltage also acts as the reference frequency of the input current, as the target is to achieve unity power factor at the input of the rectifier. Two steady-state cases have been considered where the frequency of the input voltage is 49.3 Hz and 50.7 Hz. These frequencies result in non-integer ratios between the sampling frequency and frequency of the reference signal. Initially only

¹Theoretically, the compensator should be chosen as the exact inverse of the system model to achieve zero-phase tracking error. However, practically the parameter uncertainties and load variations make it very difficult or impossible to achieve the exact inverse of the system model. The compensator in this experiment has been selected to account for practical delays occurring within the hardware. Initially the compensator was selected as a subsystem having gain = 1 and the phase difference between the reference current and actual current was measured. z^5 was found to cancel out that undesired phase difference.

Table 6.1: System parameters.

Nominal Values	Actual Values	Controller	Others
$e_{js} = 30\sqrt{2}\sin(2\pi ft \pm \theta) \text{ V}$	$e_{js} = 30 \text{ V (rms)}, \theta = 0, 2\pi/3$	$k_r = 0.005$	$U_{dcRef} = 90 \text{ V}$
$R_n = 0.5 \Omega$	$R = 0.3 \Omega$	$M = N = 2$	$\alpha_0 = 0.5$
$C_n = 1100 \mu F$	$C = 1048 \mu F$	$k_p = 0.3$	$\alpha_1 = 0.25$
$L_n = 5 \text{ mH}$	$L = 3 \text{ mH}$	$k_i = 40$	$f_{sw} = f_s = 5 \text{ kHz}$

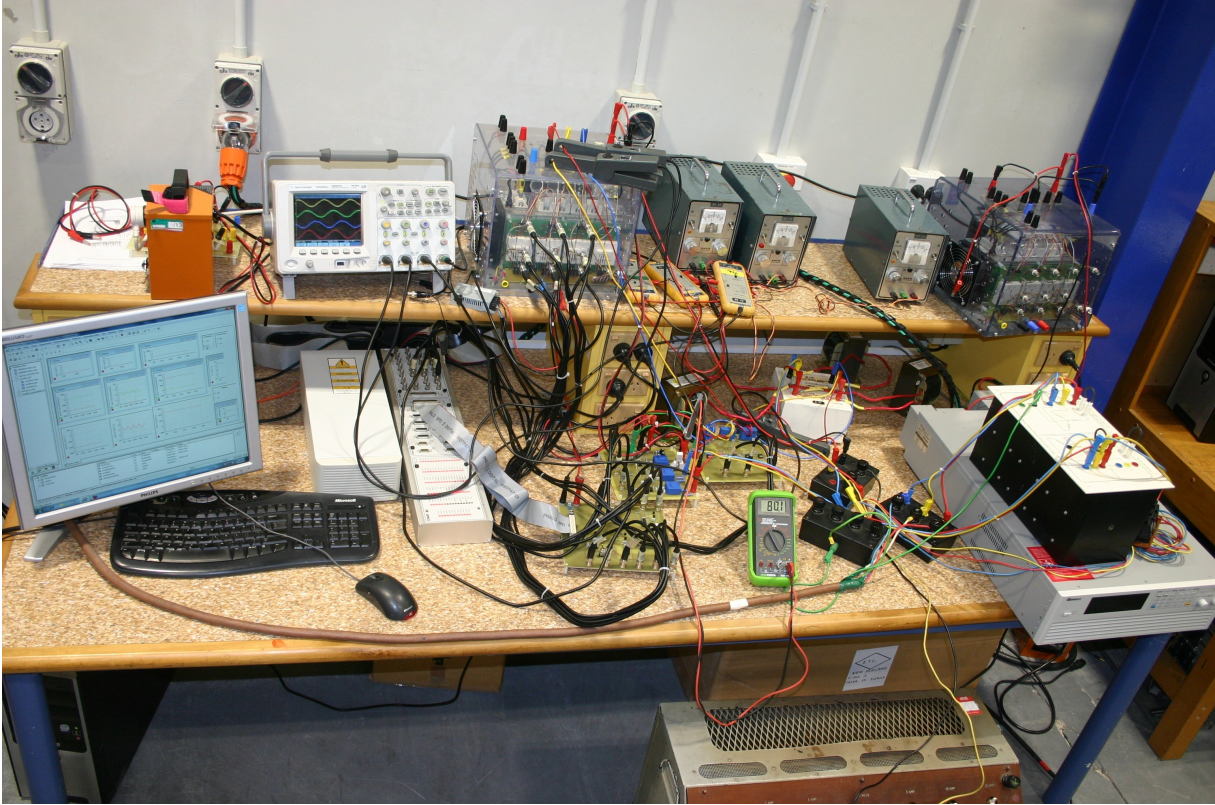


Figure 6.8: Experimental setup.

a conventional feedback controller *i.e.* a deadbeat controller has been used. The deadbeat controller operates to match the output signal in next sampling period with the reference signal in the current sampling period. It has been shown in the literature that the performance of the deadbeat controller greatly depends upon the accuracy of the model parameters. In practice, parameter uncertainties such ΔL , ΔC , ΔR_{on} and un-modelled dynamics such as dead-time and converter losses (switching, heating and others) lead to large tracking errors in deadbeat controllers. Therefore, an ARC is included to overcome the periodic disturbances, parameter variations and the issue of non-integer samples per period.

Figures 6.9 and 6.10 show the steady-state response of all three phases, of a deadbeat controlled PWM rectifier, when the frequency of the input ac signal is 49.3 Hz and 50.7 Hz respectively. The aim of this experiment is to achieve a boost dc output voltage along with low THD current and unity power factor at the input of the rectifier in the presence of frequency varying input voltage. It can be clearly seen from Figure 6.9 and 6.10 that the THD of the line current is $8\% \leq THD \leq 9\%$ (except THD of i_c at $f = 49.3$ Hz, which is far lower than the THD of other phases) in both cases and power factor is also far from unity. The THD values given here are

the average THD values of the last two cycles of steady-state measurements. The overall steady-state THD of i_c at 49.3 Hz has been found quite similar to the other two phases. However, it has been found significantly low in the cycles shown here. An advanced repetitive controller is needed to achieve unity power factor and low THD of the current.

A plug-in ARC is included in the deadbeat controlled rectifier. All the experiments have been run for 60 seconds to check both the transient and steady-state behaviors. For the ARC controlled rectifier response, an ARC controller is included in the deadbeat controlled rectifier at time $t \approx 9.75$ s when $f = 49.3$ Hz and at $t \approx 7.65$ s when $f = 50.7$ Hz. Figure 6.11 and 6.12 show the steady state response of input side voltage/current and transient response of the input current tracking error when the frequency of the input ac signal is 49.3 Hz. It can be seen that the input voltage and current are now in phase for all three phases. The THD of all three-phases has been reduced to less than 3.5%. The transient response of the current tracking error for all three phases indicate that current tracking error is reduced from 2 A (peak) to approximately 0.25 A (peak) at $f = 49.3$ Hz.

Figure 6.13 and 6.14 show the steady state response of input side voltage/current and transient response of the input current tracking error when the frequency of the input ac signal is 50.7 Hz. These Figures also show that the input current of all three phases is in phase with the voltage, leading to unity power factor. The THD of all three-phases has now been greatly reduced to less than 3.83%. The comparison of Figure 6.10 and 6.13 shows that ARC tracks the reference signal very well and results in much lower THD ($\approx 8.5\%$ to $\approx 3.5\%$). The transient response of the current tracking error for all three phases indicate that current tracking error is reduced from 2 A (peak) to approximately 0.25 A (peak) at $f = 50.7$ Hz. The transient time depends upon the control gain of the ARC controller. Higher control gain, within the stability range of the control gain parameter, leads to shorter transient time.

The steady-state current tracking error could not be further reduced in our case as even the reference current is not purely sinusoidal. The reference current depends upon two parameters: the output of the PI voltage controller and phase of the input voltage. The output of the PI controller was very slightly varying. This variation in the dc output voltage lead to a variable magnitude ac reference current. Therefore the actual current could not perfectly track the reference current. However, the steady-state error and current THD has been greatly minimized by the ARC controller. In this research work sampling frequency is always equal to the switching frequency. In case of LCL or L filter based PWM regenerative rectifiers, the filter components impose a strong effect on the bandwidth. For different sampling frequencies the system would be stable for a different range of gain values. Therefore, a simulation based optimization is required to find optimal sampling frequency. Lower switching frequencies lead to high switching ripple content in ac current of the rectifier. To reduce the switching ripple content to an acceptable limit might become very challenging in case of very low switching frequencies.

In practical grid connected converters the frequency of the reference signal varies continuously so the transient response of the converter is very important. The transient time of the controller needs to be very short. In this experiment the frequency of the reference signal is step changed from 50.7 Hz to 49.3 Hz for transient analysis. The system is already operating in steady-state conditions at $f = 50.7$ Hz *i.e* input voltage and current are in phase and output dc voltage is 90 V. The frequency is step changed from 50.7 Hz to 49.3 Hz at $t \approx 18.9$ s as shown in Figure 6.15. It is required that the frequency is continuously measured and the parameters of the ARC are calculated and updated online. However, practically the frequency of the input voltage and ARC parameters are updated based on prior knowledge and are programmed. It can be seen that the controller takes nearly 2 seconds to reach its steady-state again. Figure 6.15 shows the response of phase a only and current tracking error for all other phases are similar. The reference and actual current of phase a are given in Figure 6.16. It can be seen that inductor current of phase a tracks the reference current well in both steady-states. However, tracking error during

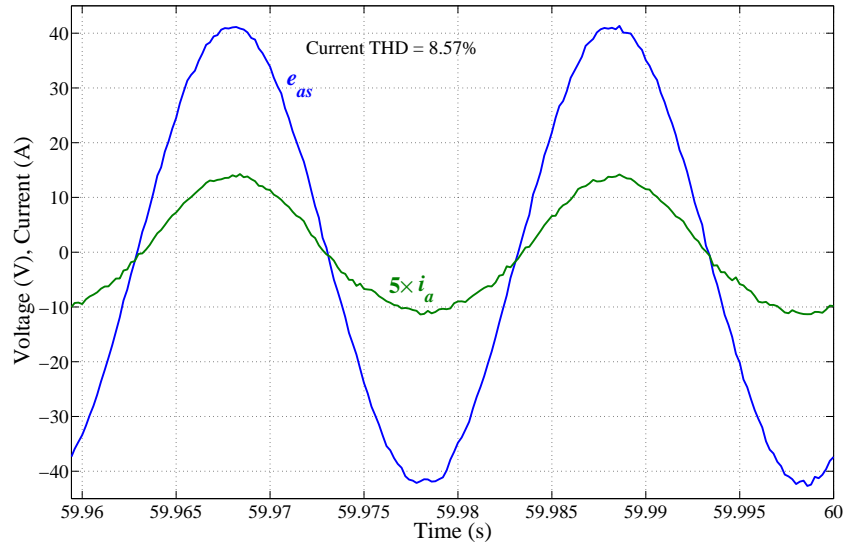
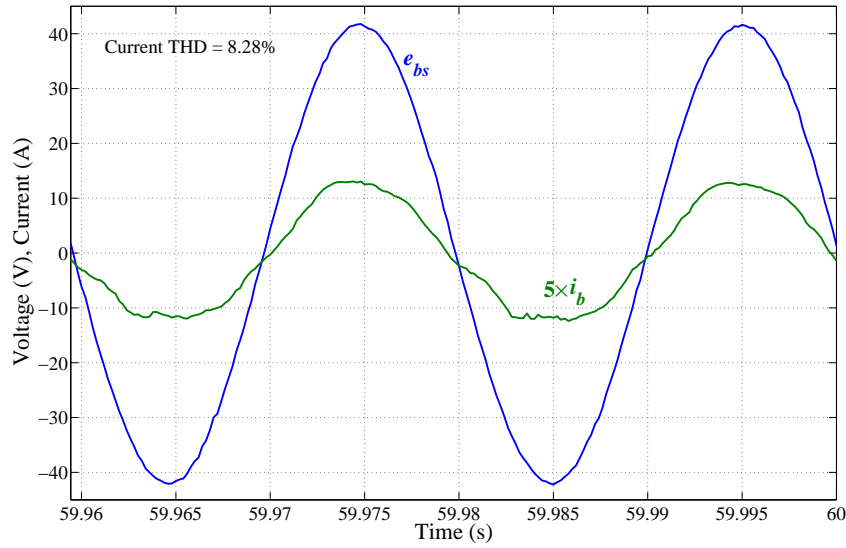
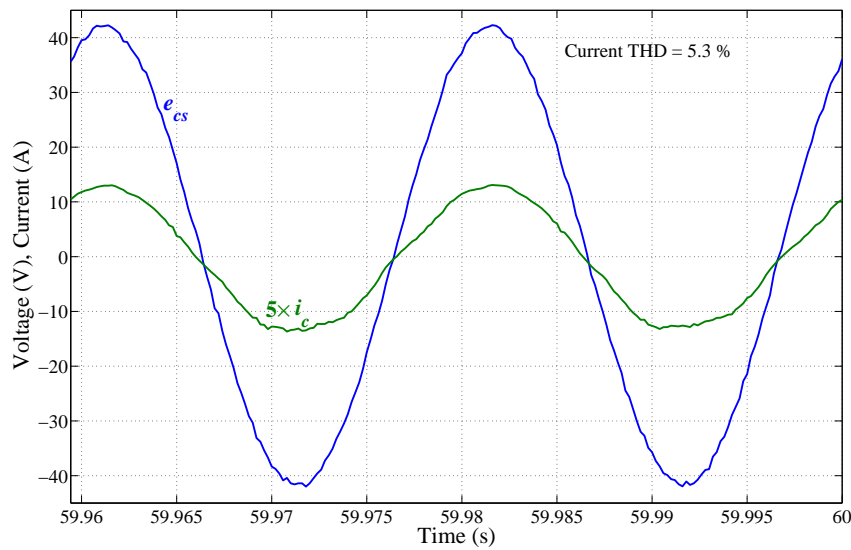
(a): Steady-state response of phase a .(b): Steady-state response of phase b .(c): Steady-state response of phase c .

Figure 6.9: Deadbeat controlled PWM rectifier's input side voltages and currents when the frequency of the reference signal is 49.3 Hz.

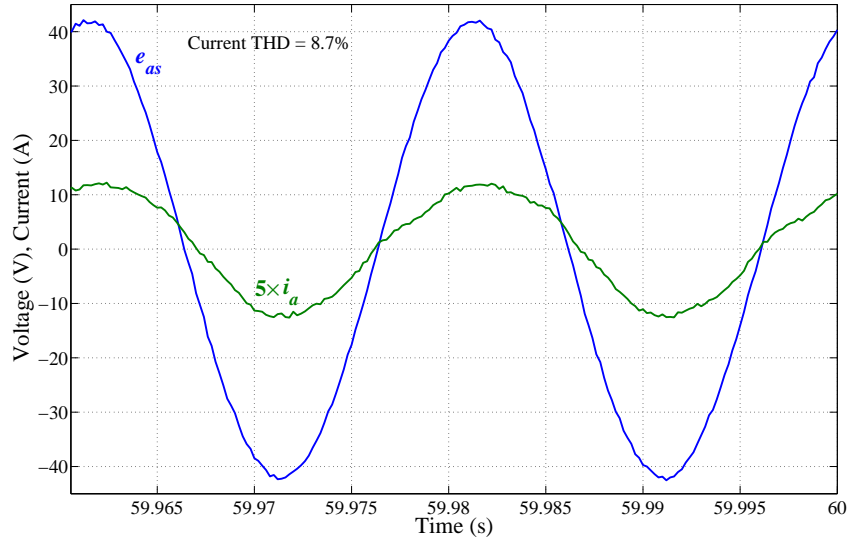
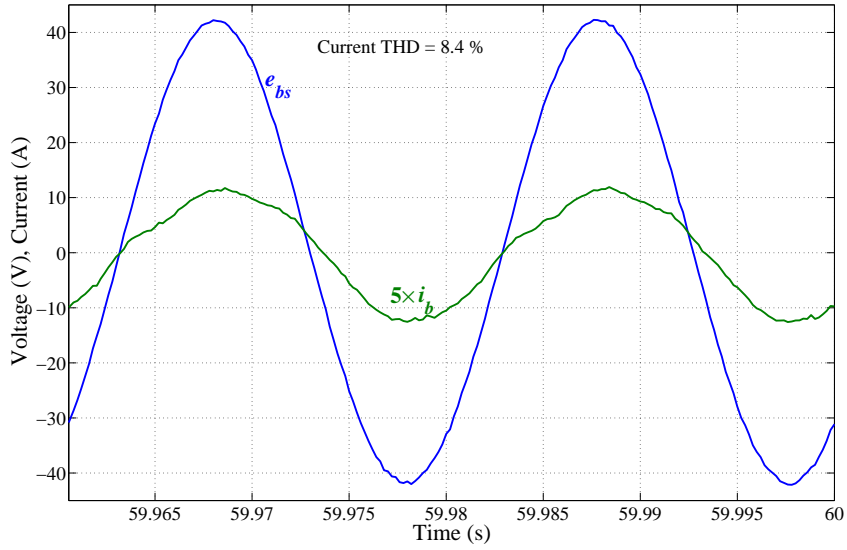
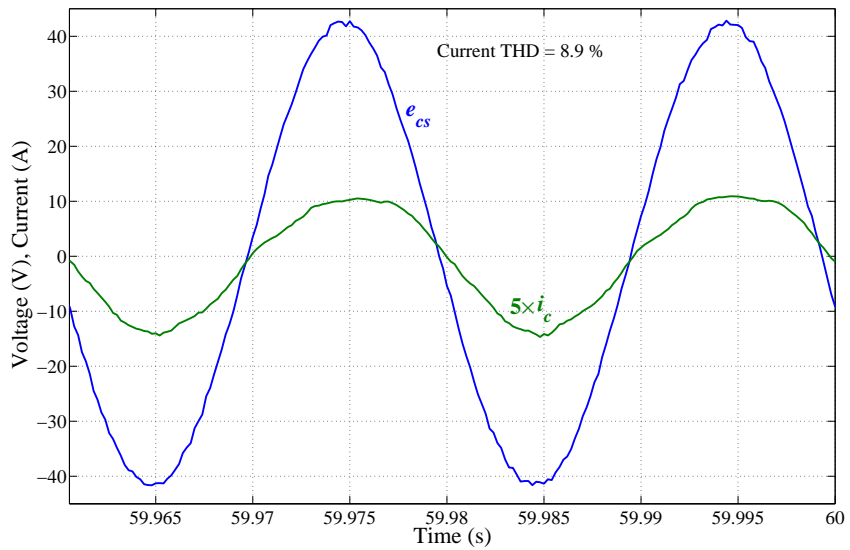
(a): Steady-state response of phase a .(b): Steady-state response of phase b .(c): Steady-state response of phase c .

Figure 6.10: Deadbeat controlled PWM rectifier's input side voltages and currents when the frequency of the reference signal is 50.7 Hz.

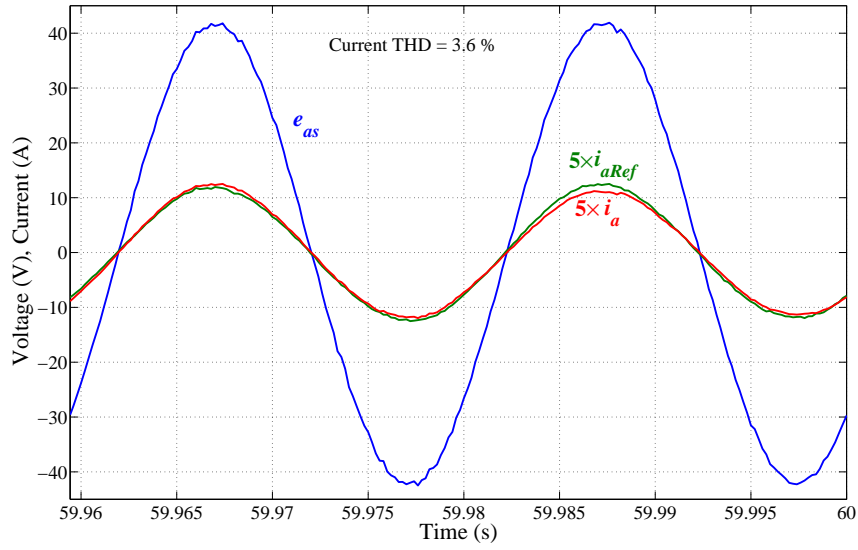
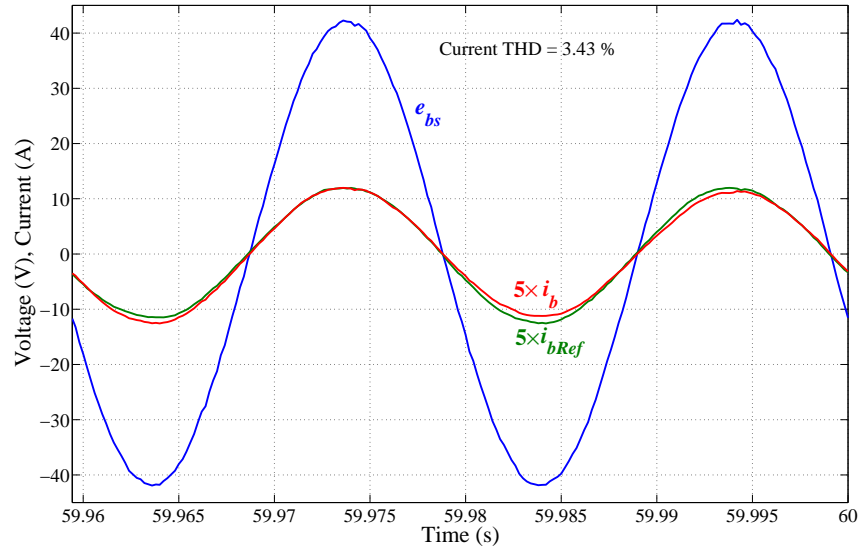
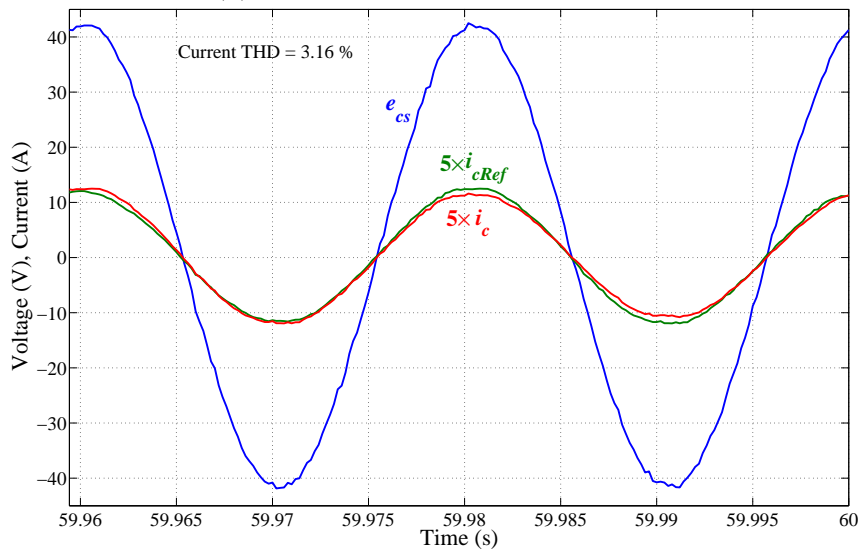
(a): Steady-state response of phase a .(b): Steady-state response of phase b .(c): Steady-state response of phase c .

Figure 6.11: Deadbeat and ARC controlled PWM rectifier's input side voltages and currents in steady-state when the frequency of the reference signal is 49.3 Hz.

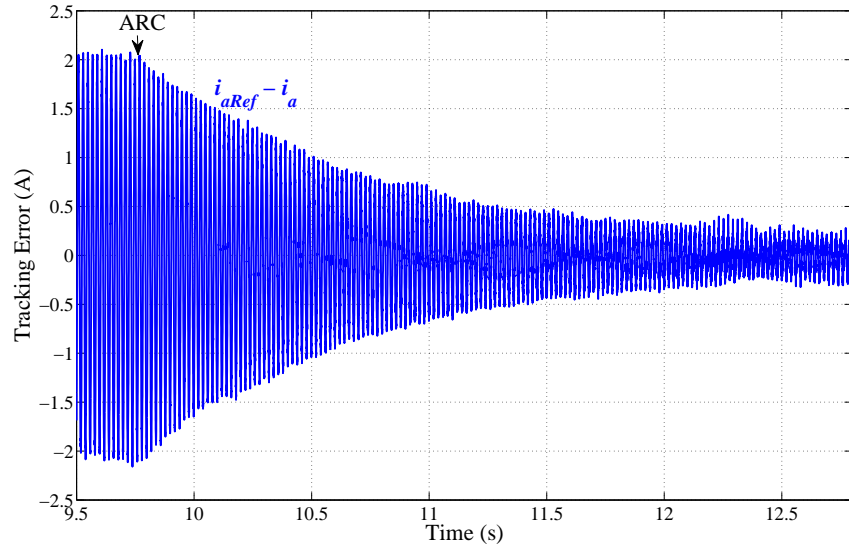
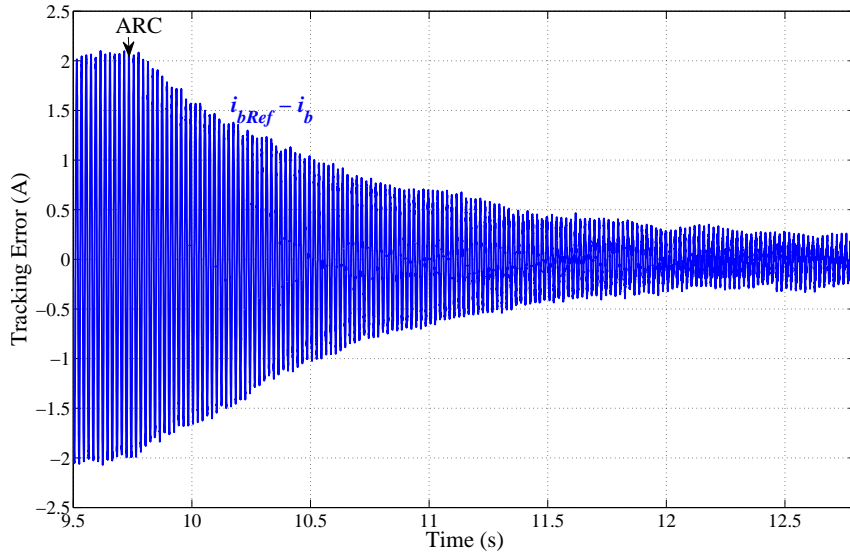
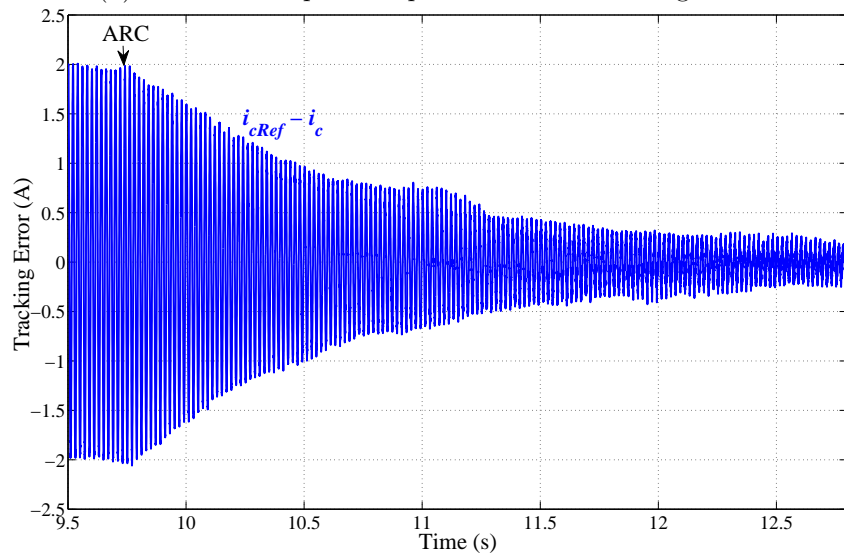
(a): Transient response of phase a current tracking error.(b): Transient response of phase b current tracking error.(c): Transient response of phase c current tracking error.

Figure 6.12: Transient response of current tracking error of all three phases when the frequency of the reference signal is 49.3 Hz.

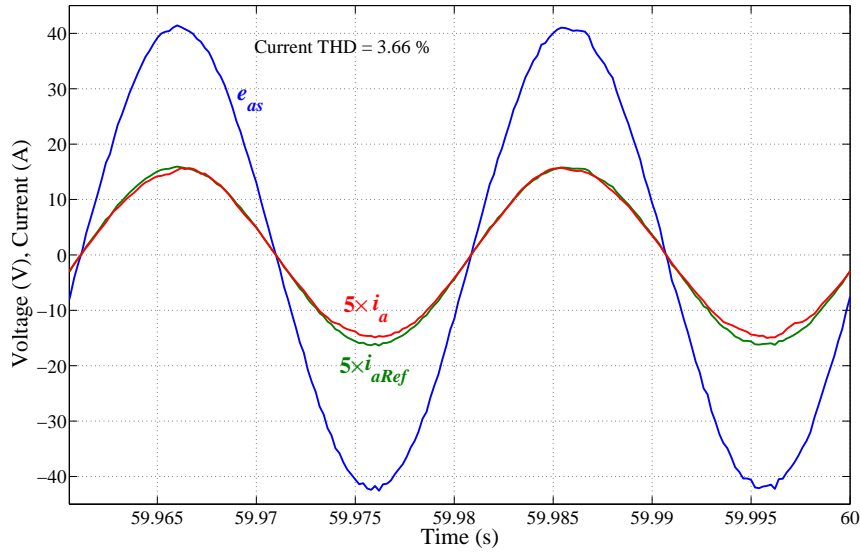
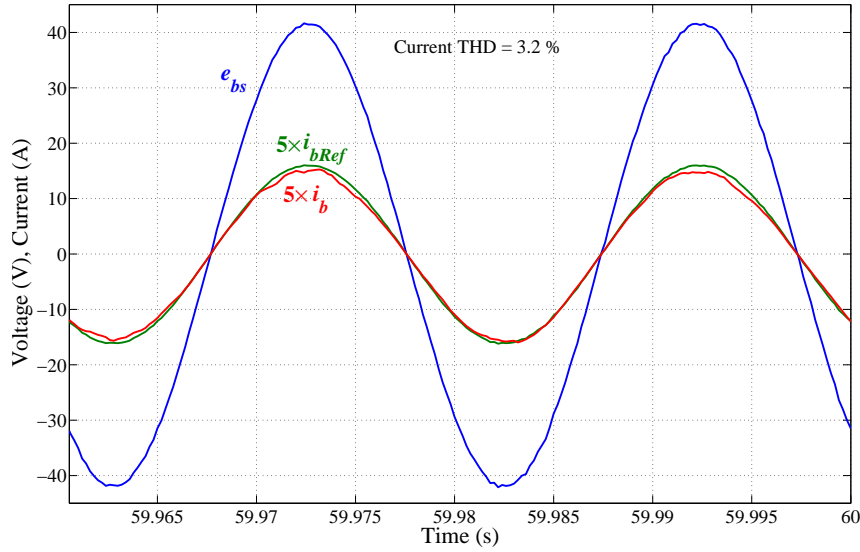
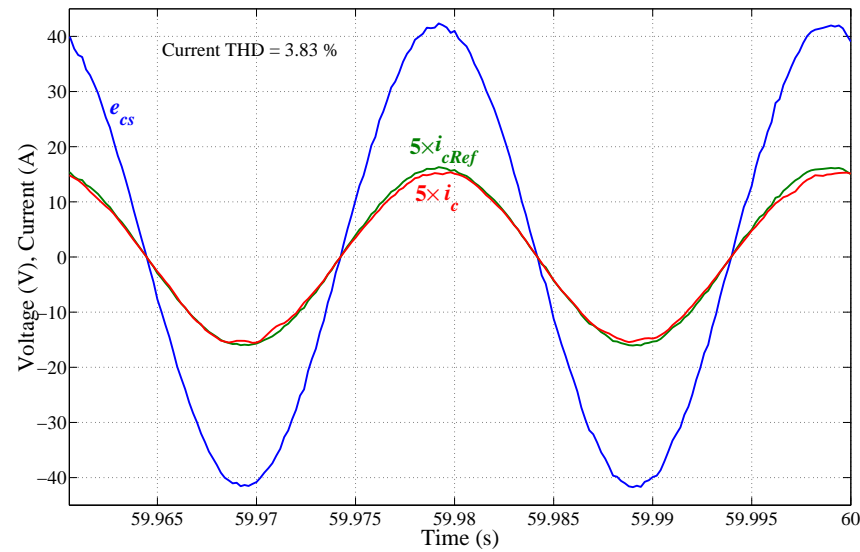
(a): Steady-state response of phase a .(b): Steady-state response of phase b .(c): Steady-state response of phase c .

Figure 6.13: Deadbeat and ARC controlled PWM rectifier's input side voltages and currents in steady-state when the frequency of the reference signal is 50.7 Hz.

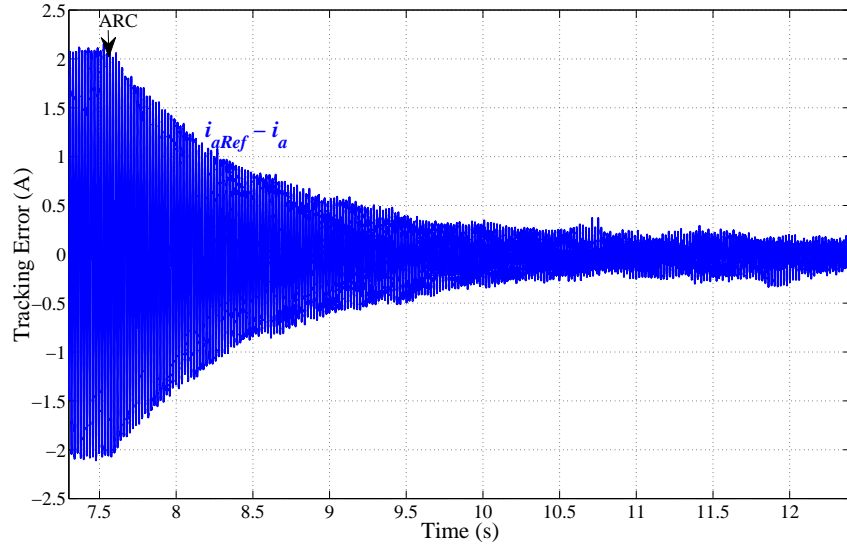
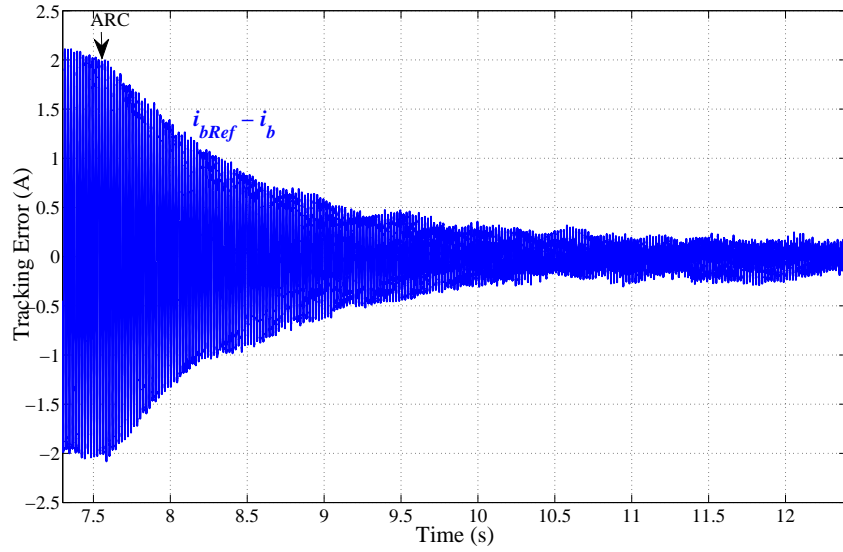
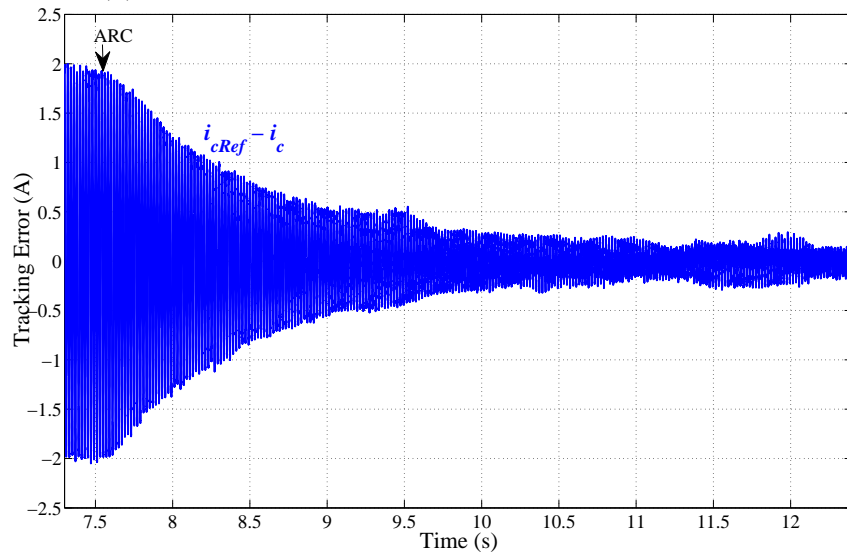
(a): Transient response of phase a current tracking error.(b): Transient response of phase b current tracking error.(c): Transient response of phase c current tracking error.

Figure 6.14: Transient response of current tracking error of all three phases when the frequency of the reference signal is 50.7 Hz.

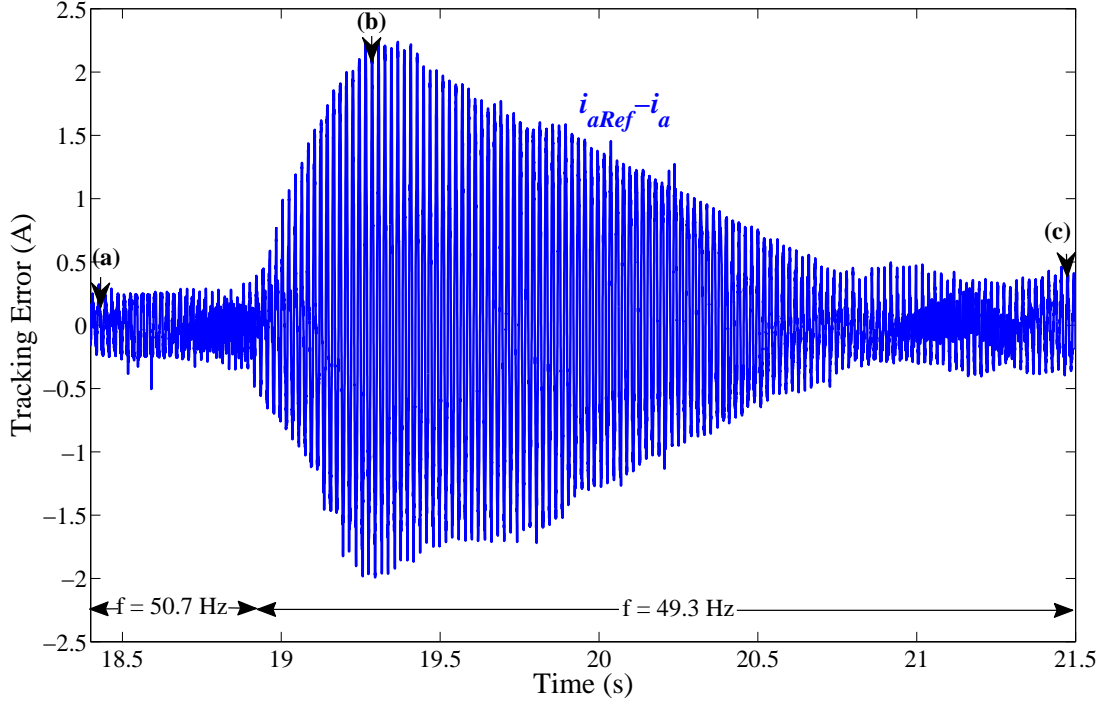


Figure 6.15: Transient response of the current tracking error ($i_{aRef} - i_a$) of phase a during frequency variations.

transient time is very big due to huge phase difference between the two signals. The step change in frequency introduced during this experiment (50.7 Hz to 49.3 Hz) is quite challenging. Under normal operation of a power system variation in frequency is much less than this. The normal rate of frequency variation in New Zealand is 0.1 Hz/s. Instantaneous frequency variation of 1.4 Hz can only occur during events of major faults. It can be concluded that if the frequency is continuously varying at 0.1 Hz/s and the transient time of the controller is 2 s, the controller would always be operating in transient state. Therefore, the controller needs to be fine tuned to further reduce its transient time. Figure 6.16 shows the details of Figure 6.16 at three different points: when the system is initially in steady-state, during transient state when the frequency is varied from 50.7 Hz to 49.3 Hz, and after reaching a steady-state again at $f = 49.3$ Hz. It can be seen that during transient state the phase difference between the reference and the actual signal fluctuates quite a lot.

6.5 CONCLUSION

In this chapter, the ARC has been used to control a three-phase grid connected PWM rectifier. A PI controller has been used to achieve the boosted dc output voltage. However, a conventional feedback controller and an advanced repetitive controller are used together to track a variable frequency reference signal. Use of advanced repetitive controller significantly reduces the THD and tracks the reference signal with greatly reduced steady-state error thus achieving nearly unity power factor at input side. Proper initialization of the advanced repetitive controller also alleviates the risk of current overshoot during turn on process.

Finally, experimental results obtained with a laboratory prototype of three-phase grid connected rectifier have validated the advanced repetitive control scheme's ability to work well under practical variable frequency conditions *i.e.* grid connected systems.

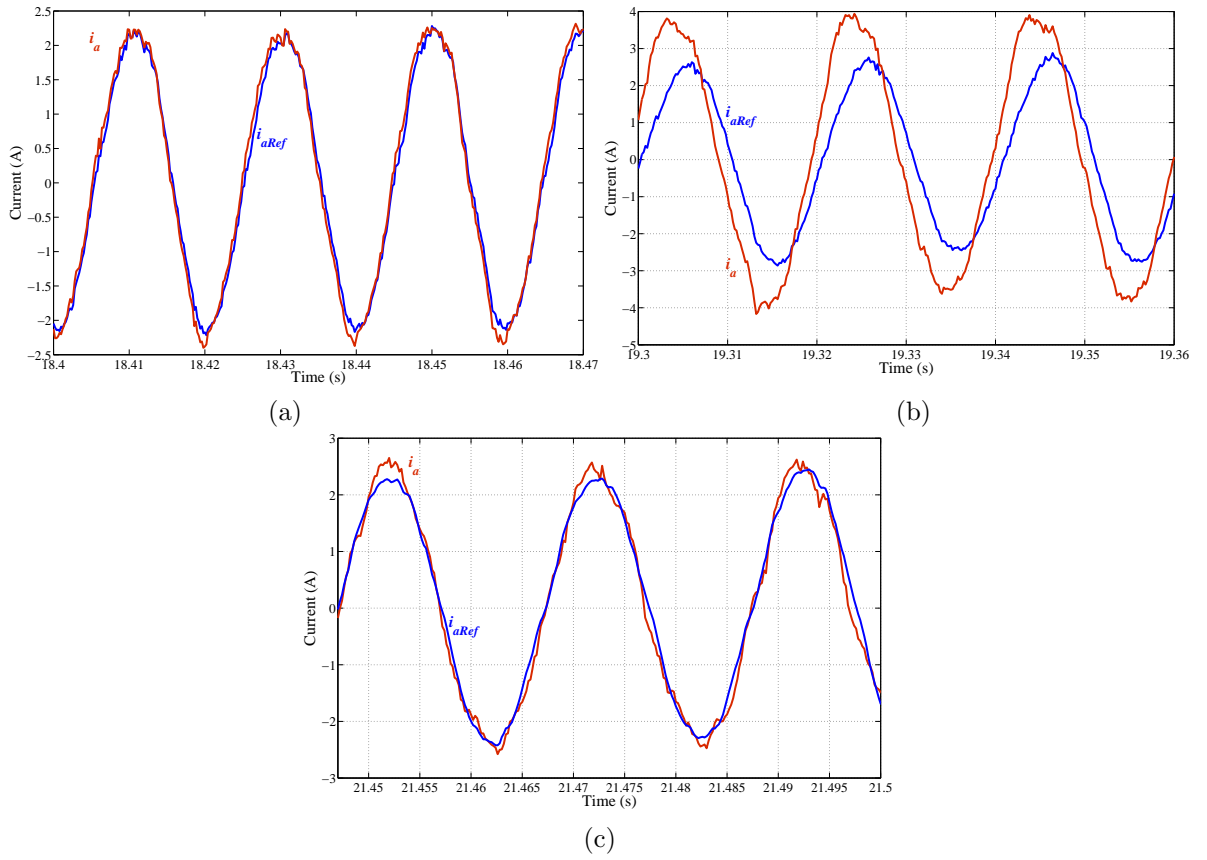


Figure 6.16: Current of phase a at different times (a) steady-state $f = 50.7$ Hz, (b) transient state $f = 49.3$ Hz, (c) steady-state $f = 49.3$ Hz.

Chapter 7

CONCLUSION AND FUTURE WORK

7.1 CONCLUSION

A wide variety of control systems deal with periodic signals. These periodic signals either act as a reference signal or disturbance. The control systems dealing with periodic signals can be divided into two categories: periodic signals with variable frequency and fixed frequency periodic signals. The variable frequency periodic signals may experience frequency variations due to the system's internal characteristics or abnormal/exceptional functioning. Repetitive control has been proven to be a zero steady-state error solution for periodic signal with constant frequency. However, performance of the repetitive controller (RC) degrades significantly when the frequency of the reference signal is not exactly known or varies with time. This thesis contributes to the topic of "performance of repetitive control working under variable frequency reference signals conditions". These contributions are summarized as follow:

- A design enhancement method and stability criteria of the Fractional Order Repetitive Controller (FORC) have been established. FORC employs a Lagrange interpolation based Fractional Delay (FD) filter inside the internal model of the conventional repetitive controller and provides satisfactory performance in the presence of a variable frequency reference signal. However design modifications suggest that either only a first order fractional delay filter should be used in FORC controllers or the order of the conventional controller should be selected such that the FD filter provides delay within its optimal range and the remaining integer delay is provided by the conventional repetitive controller. The optimal delay range for a second order or higher FD filter may be greater than one sampling period. For example the optimal delay range for a second order FD filter is $F = 0.5 : 0.1 : 1.5$. In existing FORC control design methods, the delay obtained by the FD filter may not exist in its optimal delay range if the FD filter order is greater than one. Non-optimal FD filters may overestimate the magnitude of the signal and/or the phase delay response may not be constant within the bandwidth of the filter. This leads to a reduced stability range and/or higher error and increased transient time when compared to the optimal FD filters. Design enhancement using optimal FD filter offers enhanced stability range within the bandwidth of the controller.
- In grid connected converters, if the sampling frequency of the digital repetitive controller is reasonably high ($f_s > 10\text{k Hz}$) and frequency variations are small $\Delta f = \pm 0.5$, an adaptive repetitive controller (CRC_T) performs well in terms of THD and steady-state tracking error of the reference signal. Therefore, based on different applications a trade-off can be made between the computational complexity of the FORC or other computationally expensive controllers and insignificant performance variation of adaptive repetitive controller CRC_T under variable frequency conditions.

- A design method aimed at finding an RC which assures good performance and stability for a variable frequency reference signal without redesigning the FD filter is presented. The Lagrange interpolation based FD filter can be replaced with a Taylor series expansion based FD filter to alleviate the instability issues arising from the redesign of the filter. The Taylor series expansion based FD filter parameters remain unchanged (except the fractional delay parameter F) even when the reference signal frequency and hence the ratio of the sampling to reference frequency varies. The Taylor series expansion based RC has been referred to as Advanced Repetitive Controller (ARC) in this thesis. The experimental results in Chapter 5 indicate the performance and validity of the proposed ARC.
- Two experimental applications (a single-phase stand-alone inverter and a three-phase grid connected PWM rectifier) have been utilized to perform the experimental validation of the presented analysis and control strategies (FORC and ARC). The PWM rectifier has been selected as a typical application of grid connected converters and power quality at the input of the rectifier has been measured. It uses only the ARC control technique to verify performance of the ARC in real grid connected applications. The experimental results indicate that ARC works well, maintaining a satisfactory performance in terms of achieving near unity power factor at input, low current Total Harmonic Distortion (THD), tracking the reference current and obtaining a boosted dc voltage at the output.

7.2 FUTURE WORK

Grid connected converters need to track the actual grid frequency as quickly and accurately as possible. If the frequency is not measured accurately or quickly the controller might be operating to track a different signal than the actual/required. Thus the tracking error would tend to increase and may lead to instability. A research line remains untouched in this field about frequency tracking, then calculating and updating ARC controller parameters in real time. It would be interesting to investigate how quick frequency tracking, ARC parameters calculation and updating needs to be, in order to avoid the system to become unstable. Robustness of the ARC also needs to be analyzed. It can also be interesting to compare ARC with an adaptive resonant controller which on-line detected the frequency and adjusted the controller parameters. Investigation and optimization of switching and sampling frequency, L or LCL filter parameters in case of PWM rectifier and their effect on ARC control gains are also potential areas to be researched.

For ARC controllers, a suggested research side can be obtaining a better robust stability and performance trade-off. Additionally, due to the structure of the ARC controller an interesting research topic is the design enhancements of the controller providing better robustness against plant uncertainties. Because the reference frequency and thus the delay parameter F is varying the linear time varying (LTV) system framework might be a good research side for investigation, from stability analysis and transient behavior point of view.

Only first order RC controller has been considered throughout this research work and a higher order RC controller within the ARC may enhance the system robustness to reference frequency variations and affect the stability range. Therefore, future work may also include replacing first order RC with a higher order RC within ARC and compare the performance of the two controllers for the same plant.

Appendix A

MODELING OF THREE-PHASE AND SINGLE-PHASE PWM INVERTERS

A.1 MODELING OF A THREE-PHASE PWM INVERTER

The physical model of a three-phase inverter is shown in Figure A.1. The three-phase inverter circuit shown in Figure A.1 has six energy storage elements so six state variables (i_A , i_B , i_C , v_{12} , v_{23} , v_{31}) have been selected for the system's state-space representation. The circuit equations can be obtained by applying Kirchhoff's voltage and current laws as follow:

$$\begin{aligned}
 i_{Cn1} &= C_{n1} \frac{d(v_{12})}{dt} = i_A + C_{n3} \frac{d(v_{31})}{dt} + \frac{v_{31}}{R_{n3}} - \frac{v_{12}}{R_{n1}} & \text{KCL at node 1} & \quad (\text{A.1}) \\
 i_{Cn2} &= C_{n2} \frac{d(v_{23})}{dt} = i_B + C_{n1} \frac{d(v_{12})}{dt} + \frac{v_{12}}{R_{n1}} - \frac{v_{23}}{R_{n2}} & \text{KCL at node 2} & \\
 i_{Cn3} &= C_{n3} \frac{d(v_{31})}{dt} = i_C + C_{n2} \frac{d(v_{23})}{dt} + \frac{v_{23}}{R_{n2}} - \frac{v_{31}}{R_{n3}} & \text{KCL at node 3} & \\
 v_{Ln1} &= L_{n1} \frac{d(i_A)}{dt} = v_{ab} - v_{12} + L_{n2} \frac{d(i_B)}{dt} \\
 v_{Ln2} &= L_{n2} \frac{d(i_B)}{dt} = v_{bc} - v_{23} + L_{n3} \frac{d(i_C)}{dt} \\
 v_{Ln3} &= L_{n3} \frac{d(i_C)}{dt} = v_{ca} - v_{31} + L_{n1} \frac{d(i_A)}{dt}
 \end{aligned}$$

where v_{Ln1} , v_{Ln2} , v_{Ln3} represent the three inductors' voltages and i_{Cn1} , i_{Cn2} , i_{Cn3} represent

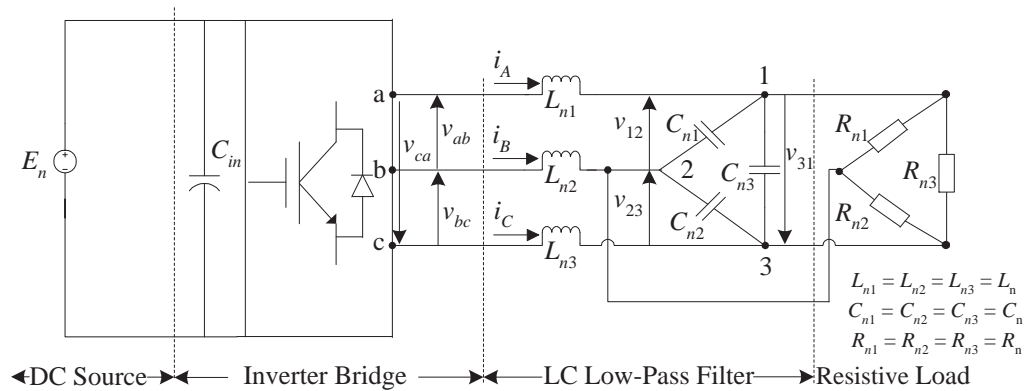


Figure A.1: Three-phase PWM inverter model

the three capacitors' currents. Since $L_{n1} = L_{n2} = L_{n3} = L_n$, $C_{n1} = C_{n2} = C_{n3} = C_n$ and $R_{n1} = R_{n2} = R_{n3} = R_n$ so (A.1) can be simplified as:

$$\begin{aligned}
 v_{12} - v_{31} &= \frac{1}{C_n} \left(i_A + \frac{v_{31}}{R_n} - \frac{v_{12}}{R_n} \right) \\
 v_{23} - v_{12} &= \frac{1}{C_n} \left(i_B + \frac{v_{12}}{R_n} - \frac{v_{23}}{R_n} \right) \\
 v_{31} - v_{23} &= \frac{1}{C_n} \left(i_C + \frac{v_{23}}{R_n} - \frac{v_{31}}{R_n} \right) \\
 i_A - i_B &= \frac{1}{L_n} (v_{ab} - v_{12}) \\
 i_B - i_C &= \frac{1}{L_n} (v_{bc} - v_{23}) \\
 i_C - i_A &= \frac{1}{L_n} (v_{ca} - v_{31})
 \end{aligned} \tag{A.2}$$

Equation (A.3) can be written in matrix form to obtain the electrical dynamics of a three-phase inverter system shown in Figure A.1.

$$\begin{bmatrix} 1 & 0 & -1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{12} \\ v_{23} \\ v_{31} \\ i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_n C_n} & 0 & \frac{1}{R_n C_n} & \frac{1}{C_n} & 0 & 0 \\ \frac{1}{R_n C_n} & \frac{-1}{R_n C_n} & 0 & 0 & \frac{1}{C_n} & 0 \\ 0 & \frac{1}{R_n C_n} & \frac{-1}{R_n C_n} & 0 & 0 & \frac{1}{C_n} \\ \frac{-1}{L_n} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{L_n} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{L_n} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{12} \\ v_{23} \\ v_{31} \\ i_A \\ i_B \\ i_C \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ \frac{1}{L_n} & 0 & 0 \\ 0 & \frac{1}{L_n} & 0 \\ 0 & 0 & \frac{1}{L_n} \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} \tag{A.3}$$

where:

v_{12} , v_{23} , and v_{31} denote the output line-to-line voltages;

v_{ab} , v_{bc} , and v_{ca} denote PWM modulated voltages;

i_A , i_B , i_C denote inductor currents;

E_n , L_n , C_n and R_n denote nominal values of dc bus voltage and components (filter inductor, filter capacitor and load resistance).

Through Clarke's 3/2 (abc to $\alpha\beta$) transformation (A.3) can be transformed to the following equation (Appendix C).

$$\begin{bmatrix} \dot{v}_\alpha \\ \dot{i}_\alpha \\ \dot{v}_\beta \\ \dot{i}_\beta \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_n C_n} & \frac{1}{3C_n} & 0 & 0 \\ \frac{-1}{L_n} & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{R_n C_n} & \frac{1}{3C_n} \\ 0 & 0 & \frac{-1}{L_n} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha \\ i_\alpha \\ v_\beta \\ i_\beta \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ \frac{E_n}{L_n} & 0 \\ 0 & 0 \\ 0 & \frac{E_n}{L_n} \end{bmatrix} \begin{bmatrix} d_\alpha \\ d_\beta \end{bmatrix} \tag{A.4}$$

The two-phase system in $\alpha\beta$ co-ordinates represented by (A.4) can be decoupled into two identical

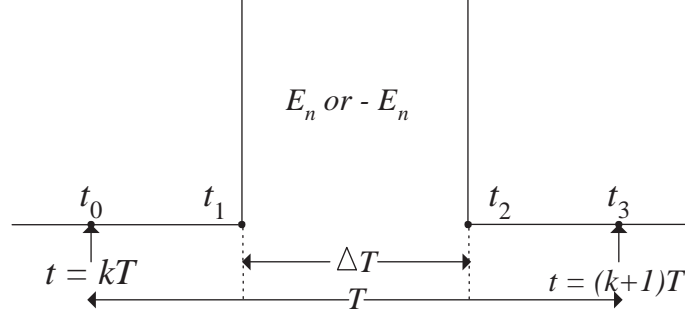


Figure A.2: One pulse of PWM pattern

independent single-phase systems as follows:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_n C_n} & \frac{1}{3C_n} \\ \frac{-1}{L_n} & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{E_n}{L_n} \end{bmatrix} \Delta T \quad (\text{A.5})$$

$$y = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

where $x_1 = v_\alpha$ or v_β , $x_2 = i_\alpha$ or i_β , $y = v_\alpha$ or v_β and $\Delta T = d_\alpha$ or d_β , d_α or d_β denote the corresponding pulse-widths in $\alpha\beta$ coordinates in one sampling interval. For a linear system, a continuous-time domain state equation is given by $\dot{x} = Ax + Bu$, where x is a state vector, u is a scalar input; A is a non-singular matrix and B is the input matrix. Its sampled-data equation can be expressed as $x(k+1) = e^{AT}x(k) + \int_0^T e^{A(T-\tau)}Bu(\tau)d\tau$. To derive the discrete model of three-phase inverter, discrete time pulse pattern shown in Figure A.2 is considered, which is the waveform of v_{ab} , v_{bc} , or v_{ca} within a sample interval T .

One cycle of the reference waveform is divided into N equal intervals of duration T . Thus the IGBT switches are turned on and off during each sampling interval T , so that the inverter voltage v_{ab} , v_{bc} , and v_{ca} becomes a pulse of magnitude $+E_n$, $-E_n$, or zero with the width ΔT centered in the interval T as shown in Figure A.2. The discrete-time domain solution for $\dot{x} = Ax + Bu$, for $0 \leq t \leq T$ is

$$x(t) = e^{At}x_0 + \int_0^t e^{A(t-\tau)}Bu(\tau)d\tau \quad (\text{A.6})$$

If the input u is constant for $0 \leq t \leq T$ then (A.6) at $t = T$ becomes:

$$x(T) = e^{AT}x_0 + A^{-1}(e^{AT} - 1)Bu \quad (\text{A.7})$$

Using (A.7) the sampled-data equation of (A.5) with the input of Figure A.2 is derived as follows:

For $0 \leq t \leq t_1$, $u = 0$ thus at $t = t_1$

$$x(t_1) = e^{At_1}x_0 \quad \text{where } x_0 \text{ is the initial state at } t = t_0 \quad (\text{A.8})$$

For $t_1 \leq t \leq t_2$, $u = E_n$ thus at $t = t_2$

$$x(t_2) = e^{A(t_2+t_1)}x_0 + A^{-1}(e^{A\Delta T} - 1)BE_n \quad (\text{A.9})$$

For $t_2 \leq t \leq (t_3 = T)$, $u = 0$ thus at $t = t_3$

$$\begin{aligned} x(t_3) &= e^{At_3} \left(e^{A(t_2+t_1)}x_0 + A^{-1}(e^{A\Delta T} - 1)BE_n \right) + A^{-1} \left(e^{A(T-\Delta T)/2} - 1 \right) B \times 0 \quad (\text{A.10}) \\ &= \left(e^{A(t_3+t_2+t_1)}x_0 + e^{At_3}A^{-1}(e^{A\Delta T} - 1)BE_n \right) + 0 \\ &= e^{AT}x_0 + e^{A(T-\Delta T)/2}A^{-1}(e^{A\Delta T} - 1)BE_n \end{aligned}$$

Using the Taylor series Approximation $e^{AT/2} \approx 1 + \frac{AT}{2} + \frac{(AT/2)^2}{2}$ and after some manipulations (A.10) becomes [115, 116]:

$$x((k+1)T) \approx e^{AT}x(kT) + e^{AT/2}BE_n\Delta T \quad (\text{A.11})$$

where $(k+1)T = t_3$ and $kT = t_0$

$$\begin{aligned} e^{AT} &\approx 1 + AT + \frac{(AT)^2}{2} \approx \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} + \begin{bmatrix} \frac{-T}{R_n C_n} & \frac{T}{3C_n} \\ \frac{-T}{L_n} & 0 \end{bmatrix} + \begin{bmatrix} \frac{T^2}{2R_n^2 C_n^2} - \frac{T^2}{6L_n C_n} & \frac{-T^2}{6R_n C_n^2} \\ \frac{T^2}{2R_n C_n L_n} & \frac{-T^2}{6L_n C_n} \end{bmatrix} \quad (\text{A.12}) \\ e^{AT/2} &\approx 1 + \frac{AT}{2} + \frac{(AT/2)^2}{2} \approx \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} + \frac{1}{2} \begin{bmatrix} \frac{-T}{R_n C_n} & \frac{T}{3C_n} \\ \frac{-T}{L_n} & 0 \end{bmatrix} + \frac{1}{4} \begin{bmatrix} \frac{T^2}{2R_n^2 C_n^2} - \frac{T^2}{6L_n C_n} & \frac{-T^2}{6R_n C_n^2} \\ \frac{T^2}{2R_n C_n L_n} & \frac{-T^2}{6L_n C_n} \end{bmatrix} \quad (\text{A.13}) \end{aligned}$$

Last matrix of the above equation is very very small, hence it can be neglected.

$$e^{AT/2}BE_n \approx \begin{bmatrix} \frac{-T}{2R_n C_n} + 1 & \frac{T}{6C_n} \\ \frac{-T}{2L_n} & 1 \end{bmatrix} \begin{bmatrix} 0 \\ E_n \\ \frac{E_n}{L_n} \end{bmatrix} \quad (\text{A.14})$$

(A.12), (A.13) and (A.14) define the sampled-data model of Figure A.1. Using the assumption $T \ll \pi\sqrt{LC}$ and the calculations given above, the sampled-data form of (A.5) becomes:

$$\begin{aligned} \begin{bmatrix} x_1(k+1) \\ x_2(k+1) \end{bmatrix} &= \begin{bmatrix} \varphi_{11} & \varphi_{12} \\ \varphi_{21} & \varphi_{22} \end{bmatrix} \begin{bmatrix} x_1(k) \\ x_2(k) \end{bmatrix} + \begin{bmatrix} g_1 \\ g_2 \end{bmatrix} \Delta T(k) \quad (\text{A.15}) \\ y(k) &= \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} x_1(k) \\ x_2(k) \end{bmatrix} \end{aligned}$$

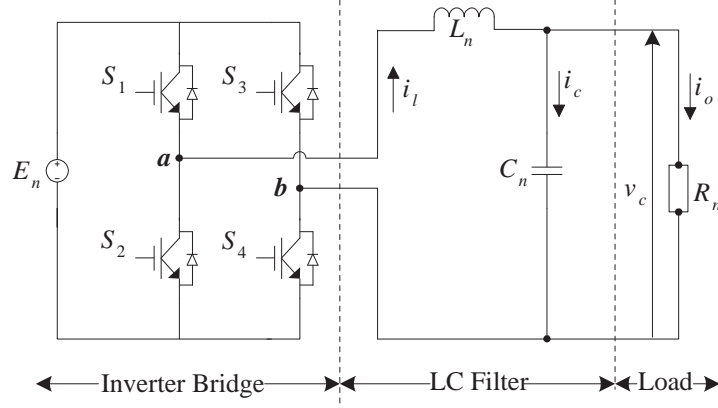


Figure A.3: A single-phase PWM inverter connected to a resistive load

where

$$\begin{aligned}
 \varphi_{11} &= 1 - \frac{T}{C_n R_n} + \frac{T^2}{2C_n^2 R_n^2} - \frac{T^2}{6L_n C_n} & \varphi_{12} &= \frac{T}{3C_n} - \frac{T^2}{6R_n C_n^2} \\
 \varphi_{21} &= \frac{-T}{L_n} + \frac{T^2}{2L_n C_n R_n} & \varphi_{22} &= 1 - \frac{T^2}{6L_n C_n} \\
 g_1 &= \frac{E_n T}{6L_n C_n} & g_2 &= \frac{E_n}{L_n}
 \end{aligned}$$

where $x_1(k)$, $x_2(k)$ and $\Delta T(k)$ represent their values at sampling instant, $t = kT$.

A.2 MODELING OF A SINGLE-PHASE INVERTER

The physical model of a single-phase inverter connected to a linear resistive load is shown in Figure A.3. It has only two energy storage elements so two state variables are required for the state-space representation (modeling) of the system.

$$C_n \frac{d(v_c)}{dt} = i_c \quad (\text{A.16})$$

$$L_n \frac{d(i_l)}{dt} = v_l \quad (\text{A.17})$$

where v_c and i_l are the state variable of the system and represent output/capacitor voltage and inductor current respectively. The circuit equations obtained by applying Kirchhoff's voltage and current laws are as follow:

$$i_c = i_l - \frac{v_c}{R_n} \quad v_{ab} - v_c = v_l = L_n \frac{d(i_l)}{dt} \quad (\text{A.18})$$

Differentiating (A.16) and substituting the value of i_c from (A.18) gives:

$$C_n \frac{d^2(v_c)}{dt^2} = \frac{d(i_l - v_c/R_n)}{dt} = \frac{1}{L_n} v_{ab} - \frac{1}{L_n} v_c - \frac{1}{R_n} \frac{dv_c}{dt} \quad (\text{A.19})$$

$$\ddot{v}_c = \frac{1}{L_n C_n} v_{ab} - \frac{1}{L_n C_n} v_c - \frac{1}{R_n C_n} \dot{v}_c \quad (\text{A.20})$$

Thus the state-space equation for the single-phase inverter system becomes:

$$\begin{aligned} \begin{bmatrix} \dot{v}_c \\ \ddot{v}_c \end{bmatrix} &= \begin{bmatrix} 0 & 1 \\ \frac{-1}{L_n C_n} & \frac{-1}{R_n C_n} \end{bmatrix} \begin{bmatrix} v_c \\ \dot{v}_c \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L_n C_n} \end{bmatrix} v_{ab} \\ y &= \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} v_c \\ \dot{v}_c \end{bmatrix} \end{aligned} \quad (\text{A.21})$$

where v_{ab} is the PWM input voltage and for unipolar PWM pulse average value of $v_{ab} = E_n \Delta T$. The system given by (A.21) is also a linear system of the form $\dot{x} = Ax + Bu$. The discrete version of the (A.21) can be achieved by considering a PWM pulse pattern given in Figure A.2 and following the same process as in case of three-phase inverter, in Section A.1 of Appendix A. Only the end results of discretization are shown here and the detailed process is skipped because it has already been explained in case of three-phase inverter.

$$x((k+1)T) \approx e^{AT}x(kT) + e^{AT/2}BE_n\Delta T \quad (\text{A.22})$$

where $(k+1)T = t_3$ and $kT = t_0$

$$e^{AT} \approx \begin{bmatrix} 1 - \frac{T^2}{2L_n C_n} & T - \frac{T^2}{2R_n C_n} \\ \frac{-T}{L_n C_n} + \frac{T^2}{2R_n C_n^2 L_n} & 1 - \frac{T}{R_n C_n} - \frac{T^2}{2L_n C_n} + \frac{T^2}{2R_n^2 C_n^2} \end{bmatrix} \quad (\text{A.23})$$

$$e^{AT/2}BE_n \approx \begin{bmatrix} 1 & \frac{T}{2} \\ \frac{-T}{2L_n C_n} & 1 - \frac{T}{2R_n C_n} \end{bmatrix} \begin{bmatrix} 0 \\ \frac{E_n}{L_n C_n} \end{bmatrix} \quad (\text{A.24})$$

Thus the sampled-data equation of (A.21) is:

$$\begin{aligned} \begin{bmatrix} v_c(k+1) \\ \dot{v}_c(k+1) \end{bmatrix} &= \begin{bmatrix} \varphi_{11} & \varphi_{12} \\ \varphi_{21} & \varphi_{22} \end{bmatrix} \begin{bmatrix} v_c(k) \\ \dot{v}_c(k) \end{bmatrix} + \begin{bmatrix} g_1 \\ g_2 \end{bmatrix} \Delta T(k) \\ y(k) &= \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} v_c(k) \\ \dot{v}_c(k) \end{bmatrix} \end{aligned} \quad (\text{A.25})$$

where

$$\begin{aligned} \varphi_{11} &= 1 - \frac{T^2}{2L_n C_n} & \varphi_{12} &= T - \frac{T^2}{2R_n C_n} \\ \varphi_{21} &= \frac{-T}{L_n C_n} + \frac{T^2}{2L_n C_n^2 R_n} & \varphi_{22} &= 1 - \frac{T}{C_n R_n} - \frac{T^2}{2L_n C_n} + \frac{T^2}{2C_n^2 R_n^2} \\ g_1 &= \frac{E_n T}{2L_n C_n} & g_2 &= \frac{E_n}{L_n C_n} - \frac{E_n T}{2L_n C_n^2 R_n} \end{aligned}$$

where $x_1(k)$, $x_2(k)$ and $\Delta T(k)$ represent their values at sampling instant, $t = kT$. For a bipolar PWM pulse the average value of $v_{ab} = TE_n(\frac{2\Delta T}{T} - 1)$ which results in slightly different parameters $g_1 = \frac{T^2}{2L_n C_n}$ and $g_2 = \frac{T}{L_n C_n} - \frac{T^2}{2L_n C_n^2 R_n}$ and input being $v_{ab}(k)$ instead of $\Delta T(k)$ in (A.25).

ALTIUM BASED CIRCUIT DIAGRAMS OF VOLTAGE/CURRENT CONDITIONING AND PWM CONTROL BOARD



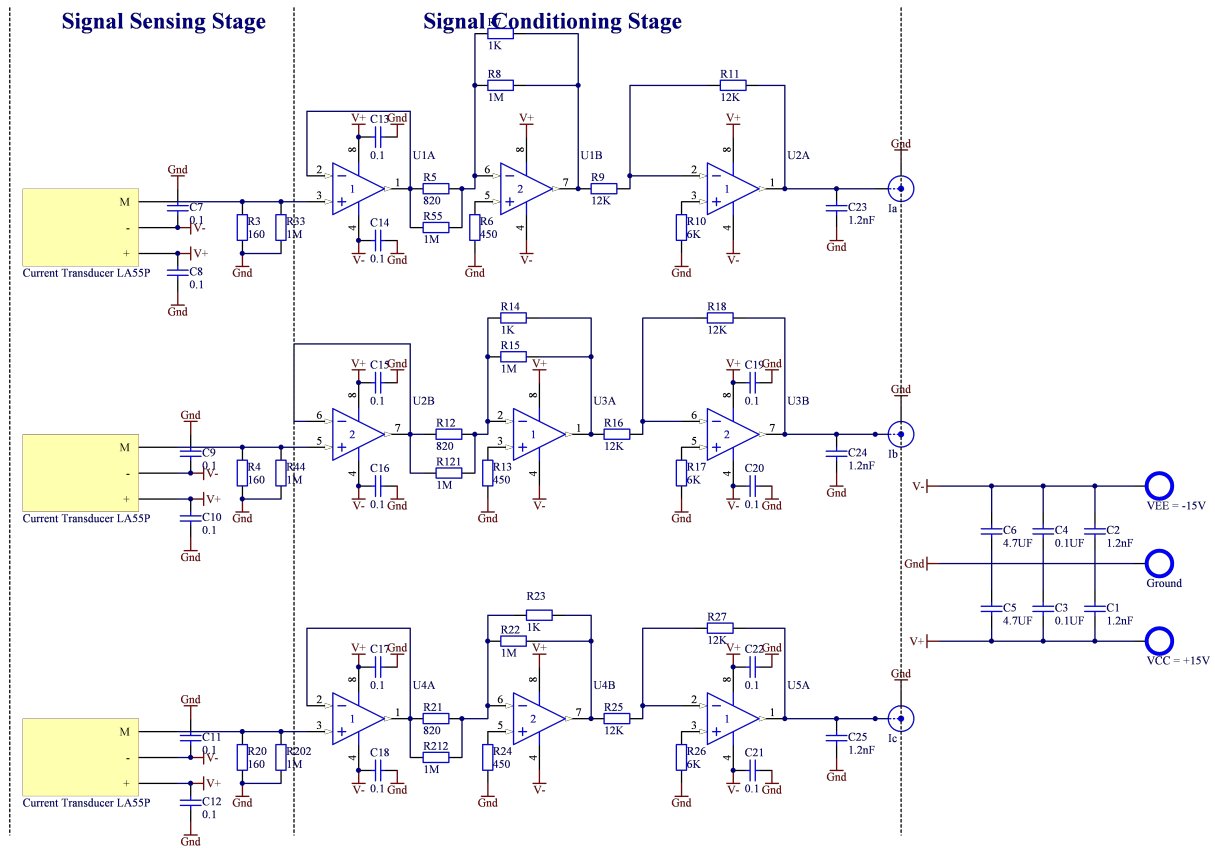


Figure B.2: Current conditioning circuit board

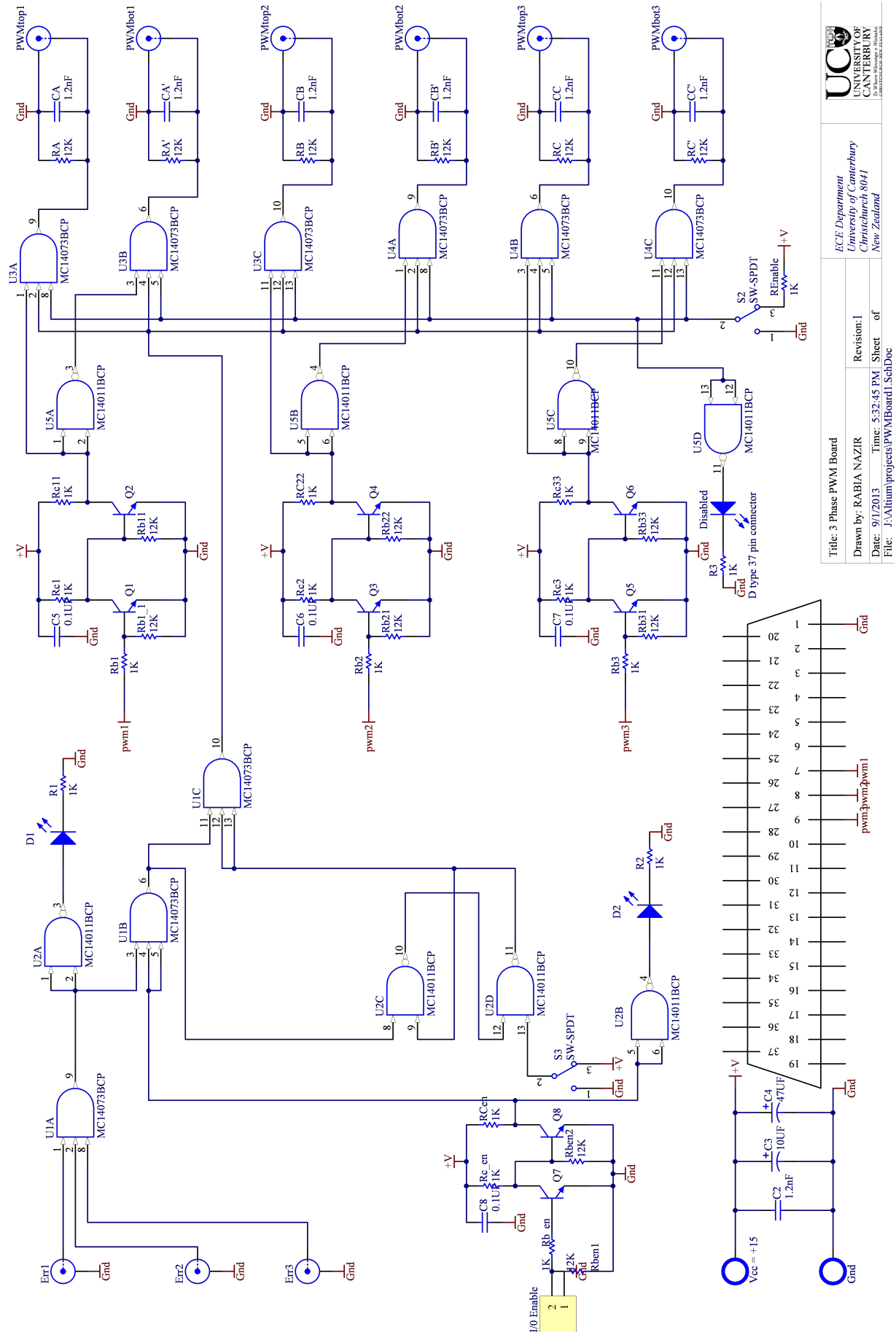


Figure B.3: Three-phase PWM control board

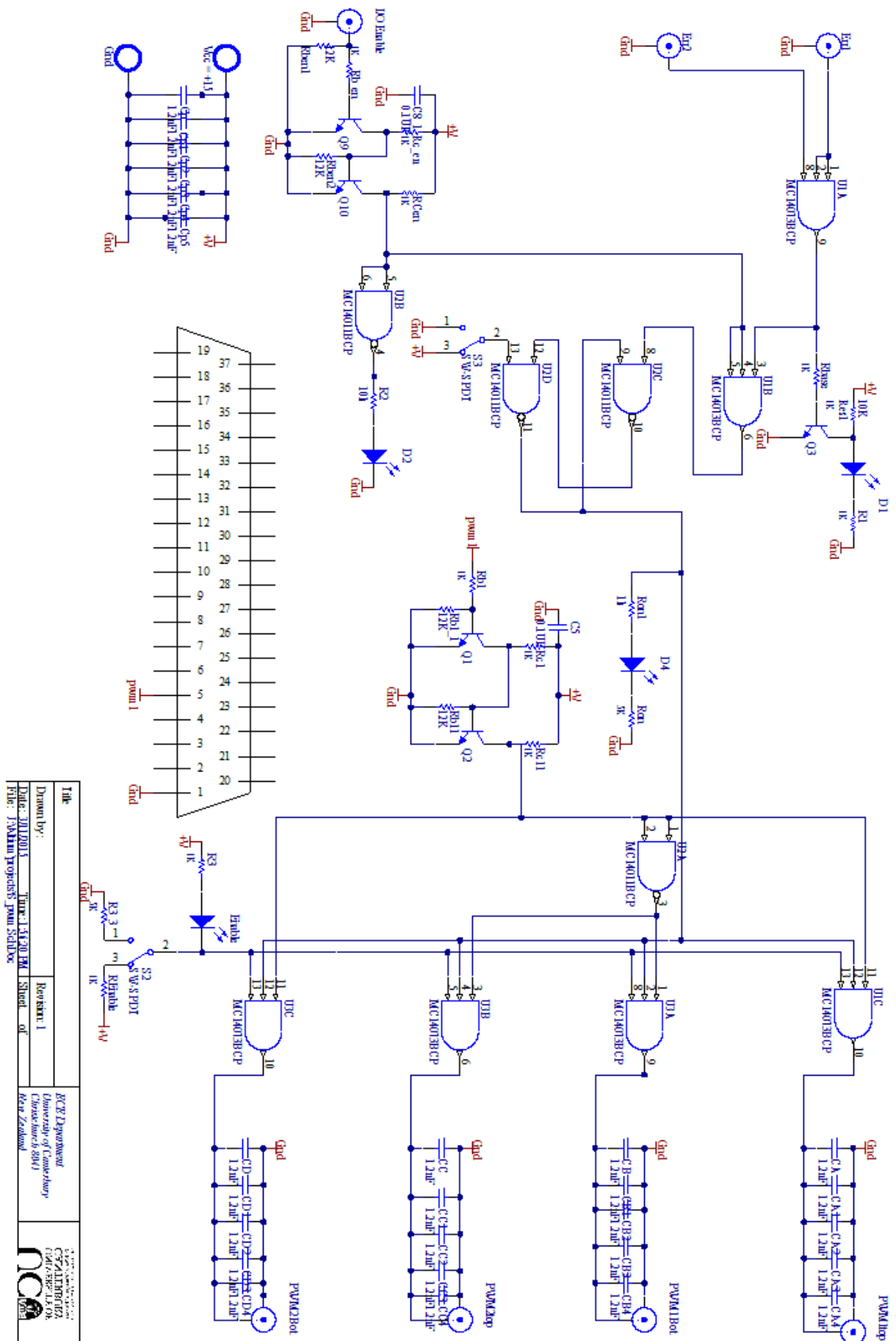


Figure B.4: Single-phase PWM control board

Appendix C

ABC TO ALPHA BETA CONVERSION

The electrical dynamics of a three-phase PWM inverter have been described in Appendix A by A.3 as:

$$\begin{bmatrix} 1 & 0 & -1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{12} \\ v_{23} \\ v_{31} \\ i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_n C_n} & 0 & \frac{1}{R_n C_n} & \frac{1}{C_n} & 0 & 0 \\ \frac{1}{R_n C_n} & \frac{-1}{R_n C_n} & 0 & 0 & \frac{1}{C_n} & 0 \\ 0 & \frac{1}{R_n C_n} & \frac{-1}{R_n C_n} & 0 & 0 & \frac{1}{C_n} \\ \frac{-1}{L_n} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{L_n} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{L_n} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{12} \\ v_{23} \\ v_{31} \\ i_A \\ i_B \\ i_C \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ \frac{1}{L_n} & 0 & 0 \\ 0 & \frac{1}{L_n} & 0 \\ 0 & 0 & \frac{1}{L_n} \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} \quad (C.1)$$

The Clarke's (3/2) transformation (abc to $\alpha\beta$) can be used to transform three-phase system of equation to a simplified two-phase system. To convert (C.1) to two-phase ($\alpha\beta$) system equation, it can be split into three parts R , S and T where $R = S + T$ and all three parts of the equation have been separately transformed using (abc to $\alpha\beta$) conversion.

$$R = \begin{bmatrix} 1 & 0 & -1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{3}{2} & \frac{-\sqrt{3}}{2} & \frac{3}{2} & 0 & 0 & 0 \\ 0 & \sqrt{3} & 0 & 0 & 0 & 0 \\ \frac{-3}{2} & \frac{-\sqrt{3}}{2} & \frac{3}{2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & \frac{-1}{2} & \frac{\sqrt{3}}{2} & 1 \\ 0 & 0 & 0 & \frac{-1}{2} & \frac{-\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \\ i_\alpha \\ i_\beta \\ i_\gamma \end{bmatrix} \\ = \begin{bmatrix} 3 & 0 & 0 & 0 & 0 & 0 \\ \frac{-3}{2} & \frac{3\sqrt{3}}{2} & \frac{-3}{2} & 0 & 0 & 0 \\ \frac{-3}{2} & \frac{3\sqrt{2}}{2} & \frac{3}{2} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{3}{2} & \frac{-\sqrt{3}}{2} & 0 \\ 0 & 0 & 0 & 0 & \sqrt{3} & 0 \\ 0 & 0 & 0 & \frac{-3}{2} & \frac{-\sqrt{3}}{2} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \\ i_\alpha \\ i_\beta \\ i_\gamma \end{bmatrix} \quad (C.2)$$

$$\begin{aligned}
S &= \begin{bmatrix} \frac{-1}{R_n C_n} & 0 & \frac{1}{R_n C_n} & \frac{1}{C_n} & 0 & 0 \\ \frac{1}{R_n C_n} & \frac{-1}{R_n C_n} & 0 & 0 & \frac{1}{C_n} & 0 \\ 0 & \frac{1}{R_n C_n} & \frac{-1}{R_n C_n} & 0 & 0 & \frac{1}{C_n} \\ \frac{-1}{L_n} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{L_n} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{L_n} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \frac{3}{2} & \frac{-\sqrt{3}}{2} & \frac{3}{2} & 0 & 0 & 0 \\ 0 & \sqrt{3} & 0 & 0 & 0 & 0 \\ \frac{-3}{2} & \frac{-\sqrt{3}}{2} & \frac{3}{2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & \frac{-1}{2} & \frac{\sqrt{3}}{2} & 1 \\ 0 & 0 & 0 & \frac{-1}{2} & \frac{-\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \\ i_\alpha \\ i_\beta \\ i_\gamma \end{bmatrix} \\
&= \begin{bmatrix} \frac{-3}{R_n C_n} & 0 & 0 & \frac{1}{C_n} & 0 & \frac{1}{C_n} \\ \frac{3}{2R_n C_n} & \frac{-3\sqrt{3}}{2R_n C_n} & \frac{3}{2R_n C_n} & \frac{-1}{2C_n} & \frac{\sqrt{3}}{2C_n} & \frac{1}{C_n} \\ \frac{3}{2R_n C_n} & \frac{3\sqrt{3}}{2R_n C_n} & \frac{-3}{2R_n C_n} & \frac{-1}{2C_n} & \frac{-\sqrt{3}}{2C_n} & \frac{1}{C_n} \\ \frac{-3}{2L_n} & \frac{\sqrt{3}}{2L_n} & \frac{-3}{L_n} & 0 & 0 & 0 \\ 0 & \frac{-\sqrt{3}}{L_n} & 0 & 0 & 0 & 0 \\ \frac{3}{2L_n} & \frac{\sqrt{3}}{2L_n} & \frac{3}{2L_n} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \\ i_\alpha \\ i_\beta \\ i_\gamma \end{bmatrix} \quad (C.3)
\end{aligned}$$

$$\begin{aligned}
T &= \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ \frac{1}{L_n} & 0 & 0 \\ 0 & \frac{1}{L_n} & 0 \\ 0 & 0 & \frac{1}{L_n} \end{bmatrix} \begin{bmatrix} \frac{3}{2} & \frac{-\sqrt{3}}{2} & \frac{3}{2} \\ 0 & \sqrt{3} & 0 \\ \frac{-3}{2} & \frac{-\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix} \begin{bmatrix} \dot{v}_{d\alpha} \\ \dot{v}_{d\beta} \\ \dot{v}_{d\gamma} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ \frac{3}{2L_n} & \frac{-\sqrt{3}}{2L_n} & \frac{3}{2L_n} \\ 0 & \frac{\sqrt{3}}{L_n} & 0 \\ \frac{-3}{2L_n} & \frac{-\sqrt{3}}{2L_n} & \frac{3}{2L_n} \end{bmatrix} \begin{bmatrix} v_{d\alpha} \\ v_{d\beta} \\ v_{d\gamma} \end{bmatrix} \quad (C.4)
\end{aligned}$$

For a balanced system, the Clarke's transformation gives $v_\gamma = 0$ and $i_\gamma = 0$. It also leads to $\dot{v}_\gamma = 0$ and $\dot{i}_\gamma = 0$ thus (C.2), (C.3), (C.4) becomes:

$$R = \begin{bmatrix} 3 & 0 & 0 & 0 \\ \frac{-3}{2} & \frac{3\sqrt{3}}{2} & 0 & 0 \\ 0 & 0 & \frac{3}{2} & \frac{-\sqrt{3}}{2} \\ 0 & 0 & 0 & \sqrt{3} \end{bmatrix} \begin{bmatrix} \dot{v}_\alpha \\ \dot{v}_\beta \\ \dot{i}_\alpha \\ \dot{i}_\beta \end{bmatrix} \quad (C.5)$$

$$S = \begin{bmatrix} \frac{-3}{R_n C_n} & 0 & \frac{1}{C_n} & 0 \\ \frac{3}{2R_n C_n} & \frac{-3\sqrt{3}}{2R_n C_n} & \frac{-1}{2C_n} & \frac{\sqrt{3}}{2C_n} \\ \frac{-3}{2L_n} & \frac{\sqrt{3}}{2L_n} & 0 & 0 \\ 0 & \frac{-\sqrt{3}}{L_n} & 0 & 0 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ i_\alpha \\ i_\beta \end{bmatrix} \quad (C.6)$$

$$T = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{3}{2L_n} & \frac{-\sqrt{3}}{2L_n} \\ 0 & \frac{\sqrt{3}}{L_n} \end{bmatrix} \begin{bmatrix} v_{d\alpha} \\ v_{d\beta} \end{bmatrix} \quad (C.7)$$

Using (C.5), (C.6) and (C.7) the original equation $R = S + T$ becomes:

$$\begin{bmatrix} 3 & 0 & 0 & 0 \\ \frac{-3}{2} & \frac{3\sqrt{3}}{2} & 0 & 0 \\ 0 & 0 & \frac{3}{2} & \frac{-\sqrt{3}}{2} \\ 0 & 0 & 0 & \sqrt{3} \end{bmatrix} \begin{bmatrix} \dot{v}_\alpha \\ \dot{v}_\beta \\ \dot{i}_\alpha \\ \dot{i}_\beta \end{bmatrix} = \begin{bmatrix} \frac{-3}{R_n C_n} & 0 & \frac{1}{C_n} & 0 \\ \frac{3}{2R_n C_n} & \frac{-3\sqrt{3}}{2R_n C_n} & \frac{-1}{2C_n} & \frac{\sqrt{3}}{2C_n} \\ \frac{-3}{2L_n} & \frac{\sqrt{3}}{2L_n} & 0 & 0 \\ 0 & \frac{-\sqrt{3}}{L_n} & 0 & 0 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ i_\alpha \\ i_\beta \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{3}{2L_n} & \frac{-\sqrt{3}}{2L_n} \\ 0 & \frac{\sqrt{3}}{L_n} \end{bmatrix} \begin{bmatrix} v_{d\alpha} \\ v_{d\beta} \end{bmatrix} \quad (C.8)$$

$$\begin{bmatrix} \dot{v}_\alpha \\ \dot{v}_\beta \\ \dot{i}_\alpha \\ \dot{i}_\beta \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_n C_n} & 0 & \frac{1}{3C_n} & 0 \\ 0 & \frac{-1}{R_n C_n} & 0 & \frac{1}{3C_n} \\ \frac{-1}{L_n} & 0 & 0 & 0 \\ 0 & \frac{-1}{L_n} & 0 & 0 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ i_\alpha \\ i_\beta \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{L_n} & 0 \\ 0 & \frac{1}{L_n} \end{bmatrix} \begin{bmatrix} v_{d\alpha} \\ v_{d\beta} \end{bmatrix} \quad (C.9)$$

Since $v_{d\alpha}$ and $v_{d\beta}$ are unipolar PWM modulated voltage so $v_{d\alpha} = E_n d_\alpha$ and $v_{d\beta} = E_n d_\beta$ where d_α and d_β are pulse-widths in one sampling interval.

$$\begin{bmatrix} \dot{v}_\alpha \\ \dot{i}_\alpha \\ \dot{v}_\beta \\ \dot{i}_\beta \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_n C_n} & \frac{1}{3C_n} & 0 & 0 \\ \frac{-1}{L_n} & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{R_n C_n} & \frac{1}{3C_n} \\ 0 & 0 & \frac{-1}{L_n} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha \\ i_\alpha \\ v_\beta \\ i_\beta \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ \frac{E_n}{L_n} & 0 \\ 0 & 0 \\ 0 & \frac{E_n}{L_n} \end{bmatrix} \begin{bmatrix} d_\alpha \\ d_\beta \end{bmatrix} \quad (C.10)$$

Appendix D

PUBLICATIONS

Following papers have been published or submitted for publication during the course of this research work.

- Rabia Nazir, Keliang Zhou, Neville R. Watson and Alan R. Wood. Analysis and synthesis of fractional order repetitive control for power converters. *Electrical Power System Research*, 124:110-119, 2015.
- Rabia Nazir, Alan R. Wood, Neville R. Watson, and Hamish Laird. Implementation of Taylor series expansion based repetitive controllers for power converters subject to fractional delays. *Automatica* (under review).
- Rabia Nazir, Keliang Zhou, Neville R. Watson and Alan R. Wood. Frequency adaptive repetitive control of grid-connected inverters. *International Conference on Control Decision and Information Technology* (CoDIT2014), 3-5 Nov. 2014. Metz, France.
- Rabia Nazir, Alan R. Wood, Hamish Laird and Neville R. Watson. Frequency adaptive repetitive control of PWM regenerative rectifiers. *International Conference on Renewable Energy Research and Applications* (ICRERA2015), (presented), 22-25 Nov. 2015. Palermo, Italy.

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